Workshop on Early Reliability Modeling for Aging and Variability in Silicon Systems - March 18th 2016 – Dresden, Germany

Opening Remarks

With the proliferation of integrated circuits implemented in the most advanced process technologies, there is a growing need to jointly analyze and understand the effect of multiple sources of failures including variability and aging early in the design cycle and their impact on system reliability. Today, conservative margins are required to ensure that devices operate correctly over their full lifetime, despite the impact of aging effects (BTI, HCI) and failure mechanisms such as EM/TDDB. New methodologies for improved cross-layer modeling and mitigation, if planned early in the design of a product, have the potential to remove unnecessary conservatism, reduce power and cost and improve yield.

The Workshop on Early Reliability Modeling for Aging and Variability in Silicon Systems (ERMAVSS) is focused on sharing new research on techniques and methodologies for modeling the effects of failures due to transistor aging, variability and other mechanisms all the way from the device level, cell level up to system level. New approaches to perform early estimations of system reliability are needed to enable reliable optimized and low-power designs.

One of the key objectives of the workshop is to foster a sharing of information between industry and researchers. For this reason, the workshop features key note talks from leading companies. A presentation by Yongsheng Sun of HiSilicon will discuss the real challenges one of the largest fabless companies is facing with regard to variability, aging and other failure mechanisms in ASICs. A talk by Rob Aitken from ARM will discuss key questions related to accuracy when analyzing the reliability of complex silicon systems. One of the industry sectors where reliability is growing in importance is automotive, and a talk by Wu-Tung Cheng of Mentor Graphics will discuss how EDA is currently providing solutions in this area. Finally, a talk by prof. Subhasish Mitra of Stanford will address how cross-layer techniques can enable significantly more efficient solutions which meet system reliability targets.

Another key goal of the workshop is to educate the audience about the latest advances in modeling the effects of variability and aging which is being achieved through a series of three embedded tutorials. The first tutorial, by Ben Kaczer of IMEC, will focus on the device level and discuss how atomic level defects in devices result in each device behaving differently over time and will discuss techniques for modeling this variability. The second tutorial, by Peter Rotter of Infineon, will discuss how aging effects can be modeled in analog circuits. The last tutorial, by prof. Ulf Schlichtmann of TUM will discuss how aging effects can be modeled at higher levels of abstraction such as gate and RT level.

A number of high-quality papers were submitted to the workshop and these will be presented as posters. The topics of these presentations cover the modeling of effects such as HCI and BTI

including how these effects can be modeled for specific types of circuits as well as how to model them at higher levels of abstraction. The selected papers after a rigorous peer-review process have been included in this volume.

Finally, in order to have a dynamic exchange and to better understand which failure mechanisms are really the most problematic, the workshop will wrap-up with a panel session to debate the question: "*Are permanent failures (EM, DB), aging failures (HCI, xBTI) and intermittent failures (radiation effects) all serious threats to the reliable operation of integrated circuits? Which class of failures poses the most serious threat to today's large integrated circuits when they are deployed in the field*?". Our panel includes speakers from IBM (Ronald Newhart), ABB (Tiberiu Seceleanu) and YogiTech (Riccardo Mariani).

We hope that the workshop will be of interest to the audience and that all participants will benefit from the expertise and knowledge of the speakers. We also hope that the format will foster interaction and a convivial atmosphere.

On behalf of the organizing committee, we would especially like to thank the numerous people who made this workshop possible. We particularly want to thank the speakers and panelists who took the time out of their busy schedules to attend and share their knowledge. We would also like to thank all the authors who have chosen this workshop to share their research. The DATE organizing committee and workshop chairs have been extremely helpful with all the logistics and planning. And we wish to thank the program committee who took the time to review the papers that were submitted.

Finally, we would like thank the two EU FP7-projects CLERECO (http://www.clereco.eu) and MoRV (https://morv-project.eu/wordpress/) for joining forces in the organization and in the sponsorship of this workshop. Both projects are conducting high quality research on reliability and ageing related topics and their strong collaboration has been one of the key factors that made the organization of such high-quality program in the workshop possible.

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