READOUT ELECTRONICS FOR TPC DETECTOR IN THE MPD/NICA PROJECT

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The article is aimed at describing the development status of the TPC front-end electronics and its design options. The TPC is placed in the middle of Multi-Purpose Detector (MPD) and provides tracking and identification of charged particles in the pseudorapidity range $|\eta| \leq 1.2$. Tracks in the TPC are registered by 24 readout chambers placed at both end-caps of the TPC sensitive volume. The readout system of one chamber consists of the front-end card (FEC) set and a readout control unit (RCU). FECs collect signals directly from the registration chamber pads, amplify them, digitize, process and transfer them to the RCU. The new design option has been motivated by the requirement of the end-cap transparency and future TPC readout chamber upgrade from multi-wire proportional chambers to GEM-chambers.

Keywords: Front-end electronics for gas detector readout; Data acquisition concepts; Time projection Chambers (TPC)

1. Introduction

The new collider complex NICA (Nuclotron-based Ion fAcility) is under active realization at the Veksler and Baldin Laboratory of High Energy Physics(VBLHEP) of the Joint Institute for Nuclear Research (JINR, Dubna) [1]. NICA facility aimed at studying heavy ion and polarized proton and deuteron collisions.

MultiPurpose Detector (MPD) will operate at one of the two intersection points of the future NICA collider [2]. The primary goal of the MPD is studying the quark-gluon plasma.

The Time-Projection Chamber (TPC) is the main tracking detector of the MPD. It has been designed for tracking and identification of charged particles [3].

2. Design concept and requirements

Drifting electron clusters from tracks induce signals on the 95232 TPC readout pads. The acquisition time is 31.2 μsec due to the maximum TPC drift time. The detector data are sampled with the rate equal to 10 MHz and measured in 10 bit ADC counts. The TPC detector data are zero dominated since the detection signal in the TPC volume appears only in the place where particle trajectories go through this volume. Therefore some kind of the data compression method should be applied.

According to the NICA collider parameters the TPC/MPD has to register the mean number of tracks equal to 300 and the maximum number of tracks equal to 1000 in the center collision at the trigger rate of 7 kHz, that will result in the mean data stream of 7 GB/s (with zero suppression). Another significant requirement is to minimize the quantity of the substance at the TPC end-caps where the front-end electronics (FEE) is located because it will shade other MPD subdetectors.

The main components of the FEE are FECs, RCUs and gigabit data links. The TPC FECs are connected to the detector pads and they process the signals generated by the charges deposited on the pads. One pad maps one readout channel. Each FEC receives data from 64 pads, digitizes them, processes, multiplexes all the information into one data stream and transfers it to the RCU through a high-speed serial link. The RCU main functions are: distribution of the trigger and clock signals to the FECs, configuration of each front-end channel and readout of the trigger related data from the FECs, subsequent formatting and transfer to the MPD DAQ system.

The readout system consists of 95232 registration channels, 1488 FECs, and 24 RCUs.

For this moment there are two design options of the TPC FEE.

3. FEC based on PASA and ALTRO chipset

The first design option is based on the ALICE TPC chipset (PASA and ALTRO) [4]. The FEC64S consists of 64 readout channels which are operating independently of each other [5]. Detector pads are directly connected to the PASA inputs. The amplified signals from the PASA chips come into the inputs of ALTRO chip where they first are digitized by a 10-bit ADC. The signal processing starts after the analogue to digital conversion. The processed and formatted data are transmitted through the parallel bus to the onboard FPGA. The main function of the FPGA is multiplexing the parallel data stream to the serial stream.

By this moment the system for 8 FECs (512 channels in total) has been prepared and tests are in progress. The FPGA development board is used as RCU prototype.

4. FEC based on SAMPA

The second design option is based on the new ASIC SAMPA [6]. The SAMPA chip was designed for the future ALICE TPC and MHC upgrade. Measurement results have shown an opportunity of designing the FEE based on the SAMPA chip also for TPC/MPD. The chip contains the analogous and digital parts in one package. More integration of the SAMPA chip allows one to make electronics of a smaller size to meet the end-cap transparency requirement. Another significant

advantage of the SAMPA is its feature to operate with input positive polarity signals as well as with negative polarity signals. This property is necessary for future upgrade of the TPC readout chambers from multi-wire proportional chambers to GEM chambers.

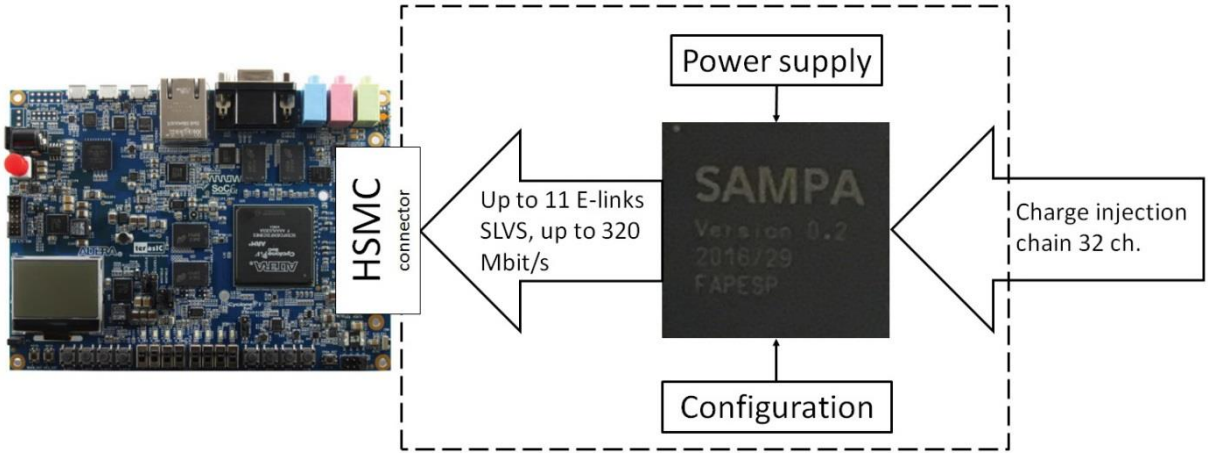

Figure 1. SAMPA test board connected to FPGA development board

The SAMPA test setup (Figure 1) consists of the SAMPA test board which is directly connected to the FPGA development board. The input charge signals are amplified and digitized by a 10-bit ADC with a sampling rate equal to 10 MHz. The digitized signal is processed by means of a digital signal processor or is not processed (depending on the selected configuration) and written to the buffer memory. After that the data stored in the channel buffer are packaged and sent to the FPGA via one of the four data links. Each of the 32 channels of the chip operates independently of each other.

Full results of the chip testing in various configurations can be found here [6].

The SAMPA test setup has allowed us to measure not only the SAMPA chip characteristics but also develop and verify FPGA firmware for the FEC based on SAMPA chip as well. For our task and requirements we have chosen the SAMPA configuration of operation in the trigger mode with a digital filter and four data links. Figure 2 shows the synchronization packet and the data packet from the SAMPA link 0 at the FPGA deserializer output. Further, the FPGA circuit filters out the data packets from the shared data stream and sends them to the FIFO buffer corresponding to each link.

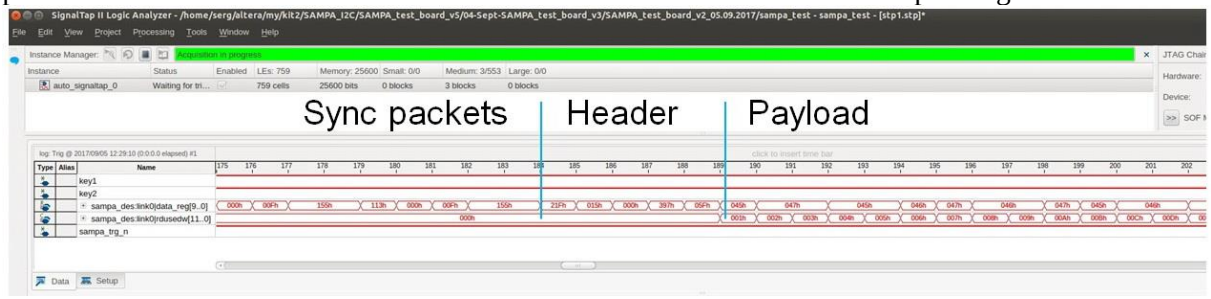

Figure 2. Deserializer output and FIFO counter waveforms captured from the logic analyzer are seen in lines 3 and 4

The developed firmware provides, first of all, the synchronization of all SAMPA links we use. After all the SAMPA links are synchronized and the synchronization packet boundary has been aligned the board is ready for triggering the data. The data packet consists of the 50-bit header (5 x 10 bit) and the 10-bit data payload.

The SAMPA FEC comprises two SAMPA chips (32 channel each), one FPGA with the embedded gigabit transceivers and other circuits (Figure 3).

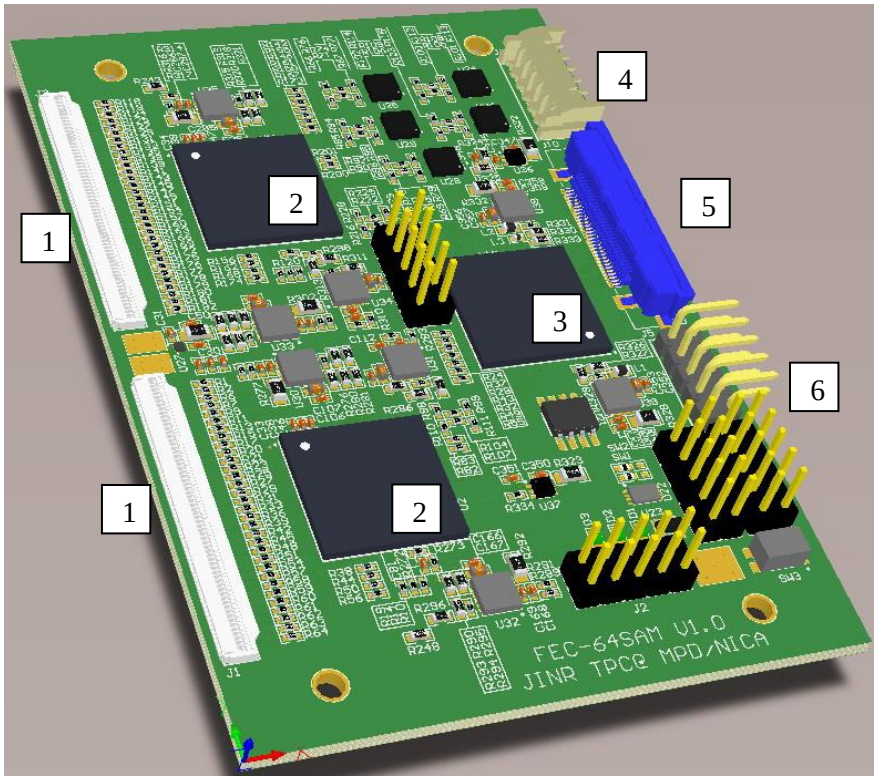

Figure 3. 3D view of the SAMPA FEC. 1 – input signal connectors, 2x32 ch; 2 – SAMPA BGA chips; 3 – configuration and board control FPGA with a gigabit transceiver; 4 – 1.7V, 3.8V, 5.0V power connector; 5 – output data connector with lines for SAMPA chip configuration, reset, clocks and triggers; 6- connectors for FPGA programming and test points

The FEC's PCB (Printed Circuit Board) contains four signal layers and four power layers divided into two supply layers and two ground layers. The FEC is 95mm wide and 65mm long.

The concept of the SAMPA based FEC has chosen similar to the FEC based on the PASA and ALTRO chipset. Our next goal is to create a system of 8 cards (512 channels in total) connected to a controller prototype based on the FPGA development board similar to the existing system based on the PASA and ALTRO chipset.

5. Conclusion

The FEE based on the PASA and ALTRO chipset provides reading out of the physical events with the mean multiplicity of 300 tracks and maximum multiplicity of 1000 tracks at the trigger rate of 7 kHz. This FEE meets all the NICA project requirements for the startup period of operation.

The FEE based on the SAMPA chip will provide all the NICA project requirements. The development of the SAMPA based FEC V1.0 has been completed. The production of the first boards is planned for the end of 2017. The work to develop the system of the 8 FECs is in progress.

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