HIGH-SPEED DATA ACQUISITION SYSTEM BASED ON DRS4 WAVEFORM DIGITIZATION

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We present a 5GSPS high-speed data acquisition system with up to 32 channels and 1024 sampling cells per channel, designed for fast-sampling, front-end applications. The data acquisition system consists of four waveform digitalization front-end circuits, one high-speed data transmission circuit and upper computer software. Waveform digitalization front-end circuit has one piece Switched Capacitor Array (SCA) chip, DRS4, developed at Paul Scherrer Institute, Switzerland. The DRS4 chip has been working in full readout mode and its eight channels are independent. High-speed data transmission circuit accept sampling data of four waveform digitization front circuits through four 2.5 Gbps serial link transceivers and send these data to upper computer real-timely. High-speed data transmission circuit with 8 lane PCI Express interface can be inserted in the PCIE x8 slot of upper computer directly and exchange data with the upper computer high-speed. Upper computer software with friendly human-computer interaction interface is responsible for system detection, sending configuration instructions, data processing and saving, etc. The first prototype of high-speed data acquisition system was designed and tested in the laboratory.

Keywords: waveform digitization, high-speed data acquisition, high-speed data transmission, switched capacitor array, DRS4, PCI Express

1. Introduction

In some high-speed particle physics experiments, there is a growing demand for high-speed sampling and digitizing detector signals, so as to realize the accurate measurement of various physical quantities, such as time, energy and pulse waveform discernment and so on [1]. Compared with the Flash ADCs and TDCs, the waveform digitization based on Switched Capacitor Arrays (SCA) has obtained the fast development because of its high sampling rate, high bandwidth, low power consumption and low cost. The basic principle is that detector signals are sampled and stored in an array of fast capacitors at a very high-speed, and digitized with a commercial ADC at a lower rate before a new waveform is acquired [2]. This technique solves the contradiction between high speed and high accuracy of analog digital transformation, and reduces the power and cost of the system by avoiding using high-speed ADC. The fourth version of Domino Ring Sampler (DRS4) is an internationally advanced waveform digitization chip form Paul Scherrer Institute (PSI) capable of sampling 9 differential input channels at a sampling speed up to 6 GSPS. Its differential inputs bandwidth is 950 MHz and power consumption is only for 140 mW typical at 2 GSPS [3]. Based on the above advantages, DRS4 is increasingly applied in high-speed particle physics experiments, such as flight time measurement[4], cosmic ray observation [5], PET scanner [6-7] and so on.

2. High-speed data acquisition system

The high-speed data acquisition system consists of four waveform digitalization front-end circuits, one high-speed data transmission circuit and upper computer software. Figure 1 shows the structure of high-speed data acquisition system. Waveform digitalization front-end circuit, the core of the data acquisition system, its main function are high-speed sampling and digitizing of analog signals, combining the data into frames, and transmitting frames to high-speed data transmission circuit through the optical fiber. High-speed digital data transmission circuit receive data from four waveform digitalization front-end circuits and send these data to upper computer through the PCI Express bus real-timely. In the meantime, high-speed digital data transmission circuit also receive instructions from upper computer and send these instructions to four waveform digitalization front-end circuits. There are 32 analog input channels of high-speed data acquisition system. Upper computer software control the whole acquisition system, such as system testing, parameter configuration, data processing and storage, etc.

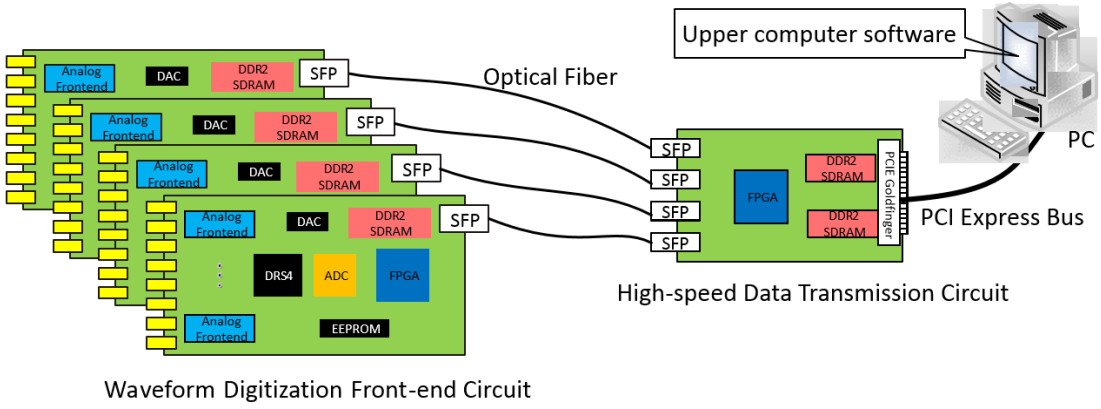

Figure 1. Structure of high-speed data acquisition system

3. Waveform Digitalization Front-end Circuit

Waveform digitalization front-end circuit is showed in Figure 2. The Circuit is based on DRS4 chip with eight analog input channels. Signals of detector through the analog front-end are

entered into the DRS4 chip in parallel. The DRS4 chip has been working in full readout mode. Eight channels are independent of each other in DRS4 chip and each channel has 1024 sampling cells. In the full readout mode, all 1024 sampling cells are read out consecutively starting from cell 0 to 1024 with clock cycles at 33 MHz. The signals of eight channels are read out in parallel into ADC, so it takes about 31 μs to read out all the data of eight channels form DRS4. The ADC has eight independent channels, all eight channels can be digitized in parallel. It means that the maximum dead time of waveform digitalization front-end circuit is 31μs. The digital data comes from ADC is exported to FPGA in parallel for combining into frames, and then cached in DDR2 memory and send out through the SFP (Small Form-factor Pluggable) interface at last. The transmission rates of SFP is 2.5 Gbps. The key parameters of the circuit are shown in table 1.

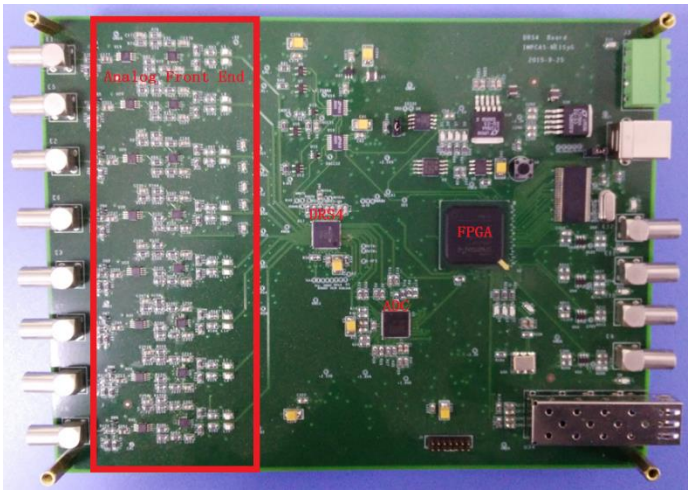

Figure 2. Waveform digitalization front-end circuit

Table 1. Key parameter of waveform digitization front-end circuit

Parameter	Value
Sampling rate	700 MSPS~5 GSPS
Input Bandwidth	≥650 MHz
Input dynamic range	1 V
DRS4 readout mode	8 channels parallel readout
Readout rate	33 MHz
ADC	14 bits
Dead time	31 μs
SFP transmission rate	2.5Gbps

4. High-speed Data Transmission Circuit

As shown in Figure 3, there are four SFP interfaces on the high-speed data transmission circuit. The transmission rates of SFP is 2.5 Gbps. The circuit has two independent DDR2 memories with 512 MB storage capacity, which can provide high-speed caching for data transmission. In order to realize high-speed data interaction with upper computer, we designed an 8-lane PCI Express interface with 16Gbps transmission rate on the circuit. We can directly insert the high-speed data transmission circuit in PCIE×8 slot on motherboard of personal computer.

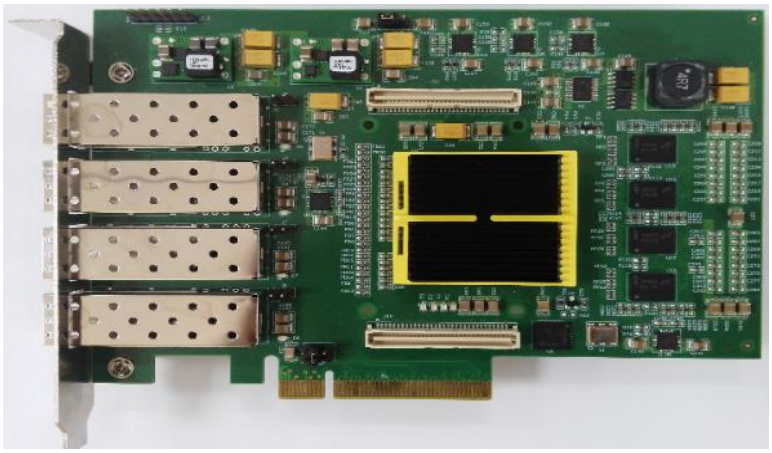

Figure 3. High-speed data transmission circuit

5. Upper Computer Software

Upper computer software is developed by c++ in the Visual Studio development environment. The PCI Express interface driver is designed by the WinDriver software [8]. Graphical user interface of software is shown in Figure 4, its major function are finding and configuring PCI Express endpoint devices, sending configuration instructions, DMA interrupt response and processing, system memory allocation and management, creating files, reading and writing hard disks, system testing, etc.

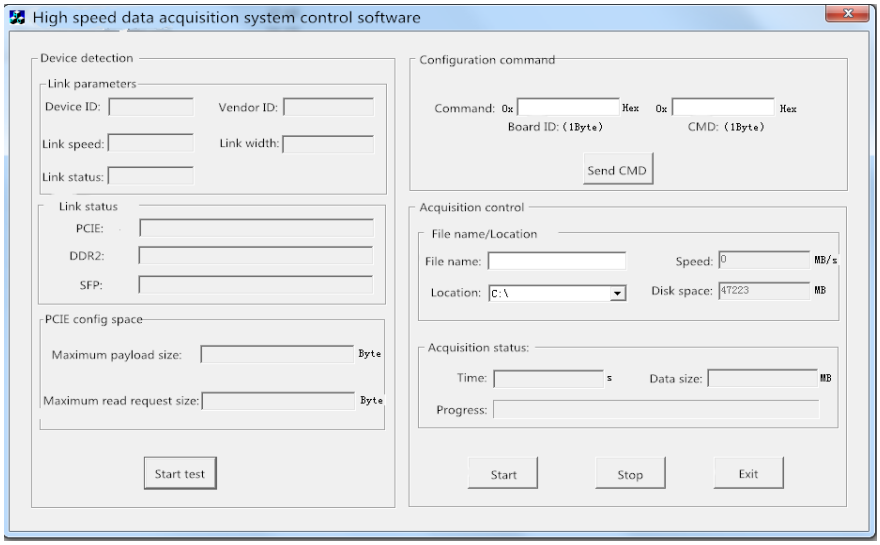

Figure 4. Upper computer software interface

6. Test results in the laboratory

The high speed data acquisition system is tested in detail in the laboratory. Results of test showed that the maximum transfer rate of SFP and PCI Express interfaces are 200 MB/s and 1598MB/s respectively, and the bit error rate are 2.147×10-12 and 2.898×10-12 respectively. We use sampling data of one of channels to test waveform reconstruction. Test signal is a sinusoidal signal, its amplitude is 225 mV and frequency is 10 MHz. Data processing result is shown in figure 5, we can get the conclusion that the system can carry out well to reconstruct the test signal by using data obtained from the actual sampling.

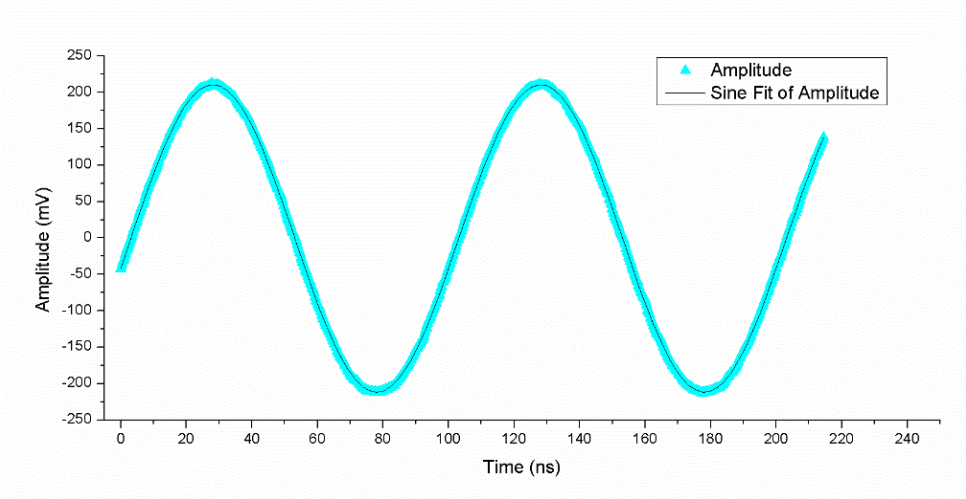

Figure 5. Reconstruction result of 10 MHz sinusoidal signal

7. Conclusion

The technology of waveform digitization based on Switched-Capacitor Arrays is increasingly applied to the particle physics experiments because of its many advantages. In this paper, the high-speed data acquisition system based on DRS4 chip has characteristics of multi-channel, high sampling rate, small dead time and long-distance transmission, thus it has generality to a certain extent.

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