Optical transceivers characteristics estimation using FPGA

Elisey Litvinov, Ivan Deyneka, and Artem Aleinik

Research Institute of Light-Guided Photonics, ITMO University,
49 Kronverksky Pr., St. Petersburg, 197101 Russia
{elitvinov,igdeyneka,artemal}@corp.ifmo.ru
http://sf.ifmo.ru/en

Abstract. The article describes the use of the FPGA board for evaluating the characteristics of optical transceivers. The main characteristics of communication lines, methods for constructing an eye diagram and jitter estimation are considered. An example of an FPGA system for evaluating the characteristics of optical transceivers is presented. An optical transceiver was evaluated and the results were obtained.

Keywords: Fiber optic network · Bit error rate · FPGA · Eye diagram · Transceivers

1 Introduction

The development of modern services of the Internet of things, 5G networks, AR and VR is impossible without increasing the bandwidth of optical communication networks. It makes the manufacturers of telecommunication equipment improve their devices and increase the supported data rate. But nowadays not only telecommunication field is searching for a high data rate solutions. Modern systems for making experiments in fundamental physics, observing the universe or developing new technologies are processing terabytes of data. Even an average laboratory could have a research project with high-speed data transfers. Most communication protocols establish strict requirements for the physical layer, as a fundamental part of the entire link. Performance of the physical layer is characterized by a Bit Error Rate (BER).In optical networks transceivers have a considerable impact on the BER. To make an optical link properly the optical transceiver with suitable bit rate, link distance and wavelength band should be used. Characteristics of each optical transceiver itself affect the entire link performance. To choose better transceiver for your application, you need to compare their performance to each other.

Transceivers characterized by an average optical power, eye-diagram coordinates, and jitter. These characteristics, as well as BER, should be measured by transferring a special bit sequence, mostly a pseudo-random bit sequence (PRBS). However, the application of the special measurement equipment to estimate optical transceivers has a number of constraints: limited types of PRBS

and a limited number of data channels; since the price of suitable equipment would be very high, it could exceed the project budget. Versatile, not expensive tools, which is capable of performing an appropriate estimation, created with available devices, are needed in a lab. For these purposes, the authors propose to use an FPGA. The FPGA contains high-speed IOs and programmable logic, which could be very useful for this application.

Until now the FPGA-based system with better characteristics compared to special measurement equipment has already been researched and developed for different spheres [1]. The FPGA-based BER tester, which was used to study the optical transceivers operation in radiation environment has been described [2]. An optical transceivers test system fully integrated into the FPGA is presented in A. Kuzmin and D. Fey research [3]. This paper also mentions the ability of FPGA to construct eye diagrams for received signals. Despite this interest, no one to the best of our knowledge has studied FPGA application to jitter estimation, which is critical for communication systems. This report aims at demonstrating the ability of jitter estimation and eye diagram construction for each data channel using the FPGA-based system. The transceivers architecture and its features enabling such estimations are briefly considered. The paper is organized as follows. The "Characteristics of a Link" section describes main link characteristics as BER, signal integrity and ways of how to estimate them. The second section gives an idea of FPGA being an estimation tool for optical transceivers. In "Application and Results" section the authors provided an example of BER testing, jitter estimation and constructing the eye diagram in the FPGA-based system.

2 Characteristics of a Link

The quality of a communication link is evaluated by the bit error rate (BER): the ratio of the number of bits received with errors to the total number of bits transmitted over the link. To get the BER value, you need to compare received data with transmitted one. Obviously, the transmitted sequence must be known at the receiving side, i.e., should be predefined. In practice, pseudo-random bit sequences (PRBS) are used, which excludes the possibility of disruption of their synchronization and evaluates real traffic.

Despite the simple definition of the BER, it is not possible to calculate the exact value of it. In practice, the BER should not exceed a certain threshold and could only be estimated. Some high-speed data protocols, like 40G Ethernet, establish the threshold better than 10^{-12}. With 95% confidence, it would take 5 minutes to pass the test if the data rate is 10 Gb/s and no errors will occur. If errors will occur, it will increase the required number of bits in order to pass the test [4].

The BERT could be used as a tool for another set of measurements, like signal integrity (SI). SI is a characteristic of the analog parameters of the communication line. Optical transceivers are the part of the communication link and perform an optoelectronic and electro-optical conversion, therefore SI of an op-

tical link straightforwardly depends on the quality of optical transceivers. One of the main measurements to analyze SI is an eye diagram of the received signal construction. An eye diagram is a type of measures aimed at visualizing and capturing the characteristics of a high-speed digital signal in the time domain. An eye diagram is a picture that repetitively displays overlapped bits waveforms during transferring the PRBS. Unlike the conventional display of a digital signal, the eye diagram does not identify individual bits within the bit pattern. However, the image of individual bits is superimposed on each other in one unit interval, which makes it convenient to visualize the quality of a digital signal. This is due to the fact that both the best and worst fronts of the signal are visualized simultaneously at the same image. Rise/fall time of a signal is also measured from the eye diagram. Usually, the eye diagram is plotted with an oscilloscope using the recorded waveforms. This method does not fit for continuous measurements, like high-speed performance analysis, due to the need to keep lots of data in memory. For this purpose, stroboscopic oscilloscopes were developed. They capture signal once at the period and plot an eye diagram from lots of points of the sample.

Next step in eye diagram technology is BERT Scan method. The BERT Scan estimates contour of the eye diagram by calculation of the BER in different points of the sample and obtains the eye diagram without analog-to-digital conversion. Different sample points mean the change of the voltage offset and the phase step of the receiver thereby it is possible to calculate BER in different points of the eye diagram. At the moments when the sample points will be around rise/fall zone (the range around the logical transition 1-to-0 or 0-to-1), the number of errors will significantly vary from one step to another.

Based on data from BERT Scan, Total Jitter (TJ) of the received signal could be estimated. Jitter is phase and frequency deviations of the transmitted signal. Jitter may be caused by instability of the oscillator, changes in the parameters of the link over time, crosstalks and other factors. It is a significant and undesired factor that has an effect on a link, in particular on PLL performance. The PLL establishes phase synchronization on the front of the incoming pulse for each bit. If this front is constantly twitching, the PLL will lose lock, and then the phase synchronization failure will begin, i.e. instead of 1, the system can read 0, instead of the N bit, the N + 1 bit. Bit errors will appear while reading the information. If the PLL can cope with the restoration of phase synchronization under the influence of jitter, then after the PLL, the jitter will be weakened greatly. The jitter amplitude is measured in given time units - unit intervals (UI). The unit interval is the time required to transmit one bit of information at a given transmission speed. TJ is a combination of several types of jitter, it is usually divided into several types or categories, depending on its properties. These properties sometimes provide information about the origin of jitter, allowing the engineer to more easily find the source of jitter.

3 FPGA as an estimation tool

In spite of programmable logic is the advantage of FPGA, modern devices include an increased portion of special function blocks with predefined, "hard" architecture. Transceivers (the high-speed IO logic blocks) are examples of these architecture blocks, they support high-speed data protocols such as 40G Ethernet, Interlaken, PCI, and others. These blocks support high-speed transfers because of their functions, which are provided by Physical Coding Sublayer (PCS) and Physical Medium Access (PMA) sublayers. The PCS compensates the phase difference between transceiver clock and the FPGA fabric clock, provides necessary coding and byte operations to satisfy protocol requirements and performs byte serialization - deserialization. The PMA performs bit serialization - deserialization, gain and equalize control of an analog signal to provide best link condition and, also, recover the clock from the received signal. Most of PMA layers have an eye diagram block, which provides an eye diagram of the received signal construction and allows to choose the best sample point position [[5], [6]]. Further, the authors consider the PMA layer blocks using a Stratix V PMA diagram as an example [7].

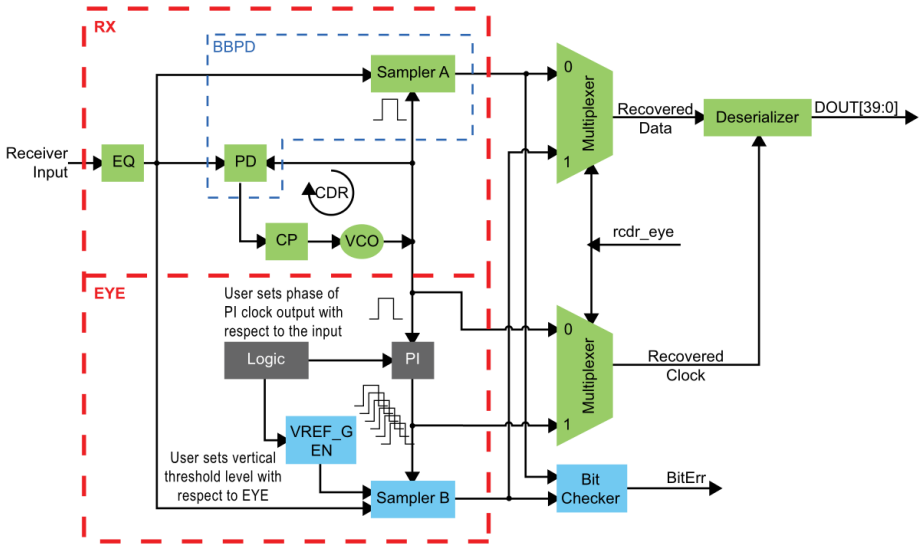

Fig. 1. Block Diagram of PMA with EyeQ feature [7]

On the received side, the signal passes an equalizer block, the task of which is to compensate for distortions that occurred during signal transmission. After adjustment, the signal hits the clock and data recovery unit (CDR). The task of this unit is to recover the clock frequency from the received signal. Based on this clock frequency, the signal is sampled over time to analyze and eye diagram

plotting. The phase interpolator (PI) uses the recovered clock frequency as a reference frequency and allows you to shift the signal sampling time by an offset of 1/32 period. The VREF_GEN block changes the voltage, according to the level of which the decision is made. Using PI and VREF_GEN, successive changes in the reference time and voltage levels in Sampler B make a decision. Based on the values of the Sampler B block and the PI and VREF_GEN shifts, the BER diagram is constructed. In addition, some of FPGAs contains a PRBS generator and checker in their transceiver blocks. If not, the PRBS generator and checker can be implemented in FPGA fabric. In this case, it is possible to generate and check any user-defined bit sequences. All of these features allow the suitable board with FPGA to be used as a stand-alone BERT.

To sum up, FPGA could act as a universal platform for BER testing, a jitter estimating, and for an eye diagram construction of the received signal.

4 Application and Results

In order to use the FPGA board for optical transceivers estimation, it is necessary to design an FPGA project and generate a firmware for the FPGA. Firmware is a program written in HDL languages. The program is synthesized, the resulted netlist placed and routed, and finally generated a file which is naturally the firmware is loaded into the FPGA. In this paper, we used Intel Quartus Prime 16.0 as a programmable logic device design software. Most of the project is carried out in QSYS - a tool for developers from Intel, which simplifies the configuration of units and their interaction with each other. The project includes several functional blocks. In order to implement and configure transceivers in FPGA Transceiver IP core should be used. There are several types of transceiver IP cores, with different communication protocol support or availability of special functions like deterministic latency. In our project Low Latency IP core was used because of its simplicity. Transceiver Reconfiguration Controller IP core provides additional functions as reconfiguring the transceiver channels to support multiple or different data rates and changing PMA settings on-the-fly or powering down the transceiver channels. To get access to transceivers from PC, Avalon MM to JTAG bridge IP core should be included into the design. It is important to pay attention to clock sources of the design. Transceiver blocks should be clocked separately from the rest part of FPGA by stable, low-jitter clock source. The Transceiver Toolkit, the plugin of Intel Quartus Prime software, is compatible with the design and could be used to make estimation easy and user-friendly.

The Stratix V Development Kit was chosen to implement the described algorithm and to perform the evaluation. The board has a QSFP+ connector for an optical transceiver and FPGA with transceivers that support rates up to 12.5 Gb/s. With the help of the built-in Quartus Prime Transceiver Toolkit the optical transceiver Finisar FTL4C1QE1C was evaluated, the results of the BER test were obtained, the jitter was estimated and the eye diagram for each of the four data channels was constructed.

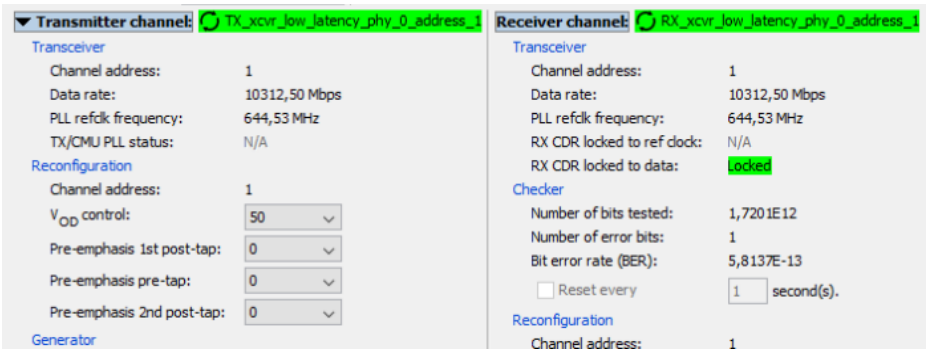

Fig. 2. BER estimation results.

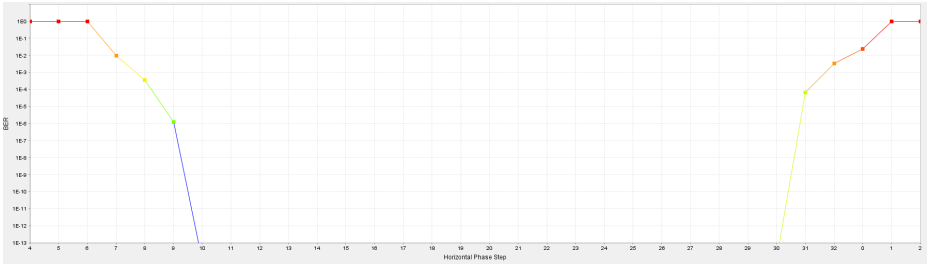

Fig. 3. Estimated BER bathtub curve.

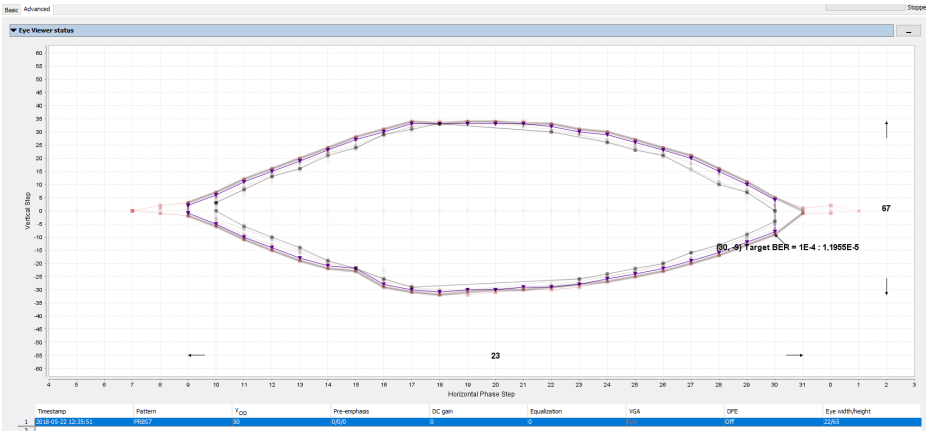

Fig. 4. Constructed eye diagram from received signal.

The estimation of the connected optical transceiver was carried out through the optical loopback with the variable fiber optic attenuator (PVOA). The PVOA was used to provide the necessary signal attenuation in order to comply with the measurement conditions and protect the receiver from destruction. The experiment showed that the tested QSFP+ met the target BER 10^{-12}. The total jitter was approximately 0.34 UI and the opening of the eye diagram was registered. As a result, the custom FPGA-based system that allows to estimate the performance and characteristics of the optical transceiver and to construct an eye diagram of the received signal was developed and tested.

5 Conclusions

The report demonstrates the use of FPGA as a universal solution in order to implement and configure transceivers. In particular, target BER 10^{-12} for QSFP+ optical transceiver Finisar FTL4C1QE1C was measured, jitter was estimated and the eye diagram for the received signal from the QSFP+ module was constructed.

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