RF Sampling of Wideband Signals Using Xilinx UltraScale+ RFSoC

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Abstract

New Xilinx RFSoC devices are very useful in modern telecommunication technology due to onboard RF data converters. Several technologies such as modern 5G or classical radar applications can benefit from that. Other advantages of using RFSoC with respect to traditional approaches are a high saving of power consumption and chip area. Since high-level development tools, such as Matlab/Simulink or High-Level Synthesis, fully support these devices, it is possible to easily implement high-bandwidth systems since modern and exploiting all RFSoC's innovative capabilities.

Keywords

Xilinx UltraScale+ RFSoC, Time Interleaved ADC, Wideband Signals, FPGA, Parallel Computing.

1. Introduction

Several applications are involved in new scenarios including satellite, rural and urban and smart city environments [1, 2, 3, 4].

Modern telecommunication technologies require an increasingly growing signal bandwidth. In this context, we can find several applications such as Digital Beam Forming Networks (DBFN), Massive MIMO (MMIMO) and Carrier Aggregation (CA) Systems. Another important example is given by newborn 5G technology that exploits a large number of channels and high data-rates. Also radio-astronomy [5, 6] or Cognitive Radio [7] applications can benefit of this technology. These signal features have required the development of new technologies by semiconductor firms with the aim to optimize the single-chip power consumption mostly focusing their effort on Radio Frequency Digital Front End (DFE/RF) [8, 9].

For instance, in the last years, Xilinx firm has placed on the market several Systems-on-Chip (SoC) equipped with new components that try to make up for the performance deficiencies of the systems already on the market. In details, the new UltraScale+ RFSoCs by Xilinx [10] are equipped with new high-speed and high-bandwidth ADC/DAC that allow to sample and reconstruct analog signals directly at RF [11] avoiding any IF down-conversion middle step as depicted in Figure 1.

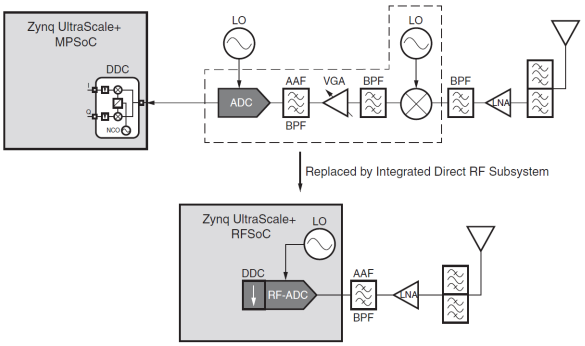

Figure 1: Classic IF down-conversion and new RFSoC approach with direct RF sampling

The main concept behind new ADCs devices is Time Interleaving (TI) sampling.

2. Time Interleaving ADCs

The TI is a technique that allows to sample high frequency signals by using more low sample-time ADC cores at the same time. Each ADC core works at $\frac{f_s}{M}$ where M is the number of ADC cores and f_s is the equivalent sample frequency of whole system. For instance, if $f_s = 1GHz$ and $M = 4$, each ADC core will work at a frequency of 250 MHz and the input signal will be sampled in different instants by each core as shown in Figure 2.

The clear advantage of this approach is the possibility to digitalize an analog signal by using a clock frequency lower than the Nyquist frequency. On the other hand, TI-ADC digital output is very sensitive to the so-called *Interleaving Spurs* (IS) [12] caused by

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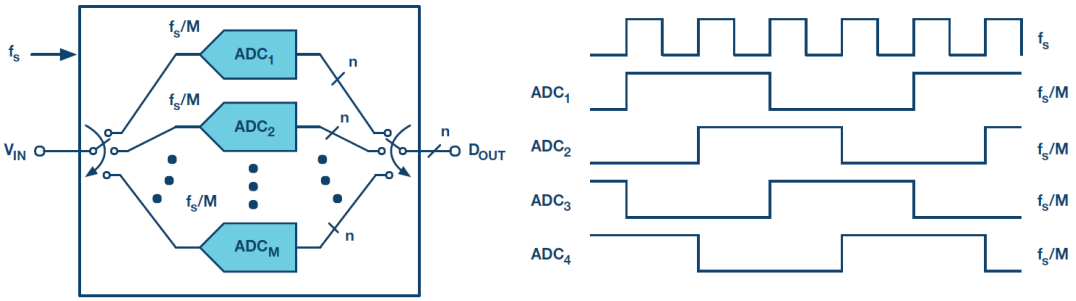

Figure 2: Operating principle of a TI-ADC

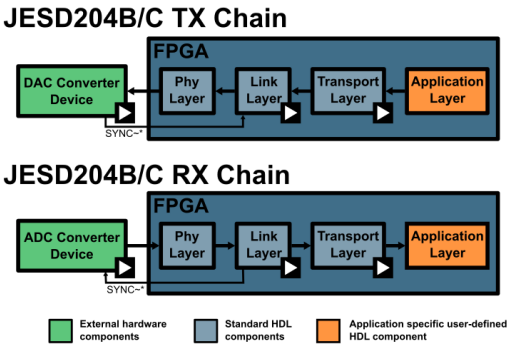

Figure 3: TX and RX JESD204 interfaces

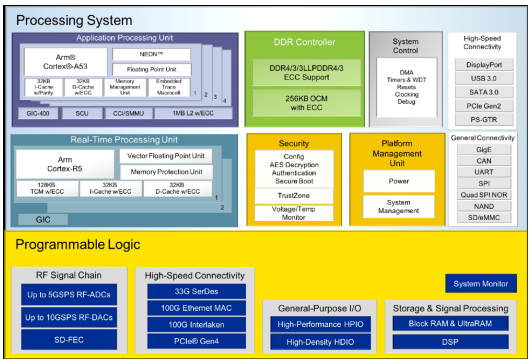

Figure 4: RFSoC block diagram

channels mismatch. The same operating principle is likewise applied to Digital to Analog Conversion (DAC) that can be adopted in [13].

3. RFSoC overview

Xilinx Zynq Ultrascale+ RFSoC is the first example of multi GS/s converters, programmable logic and ARM cortex system integration in the same SoC. It is also

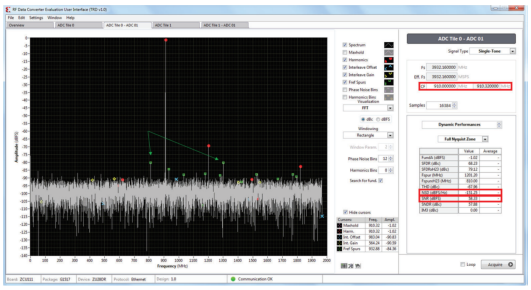

Figure 5: RF Data Converter Evaluation Tool

present a Soft-Decision Forward Error Correction (SD-FEC). The integration of these components in the same die allows to save area but mostly power (about 50%). Also the design of the board is simpler since the RF signal is directly sampled without further down-conversions. The classic approach for communicate with fast external converters exploits the JESD204 interface [14] as depicted in Figure 2 , but by integrating the converters inside the SoC, it is possible to avoid this interface with a consequent further power saving.

With current technology, RFSoC devices allow to directly sample RF signals until 6 GHz. For this reason, they are very suitable for applications using bands L, S and C:

- Multi-band networks such as 5G
- Massive MIMO
- Phased Array Radar
- Satellite communications
- Measurements instrumentation

The general block diagram of RFSoC is shown in Figure 2.

The RFSoC data conversion subsystem is composed of several RF Analog-to-digital and Digital-to-analog

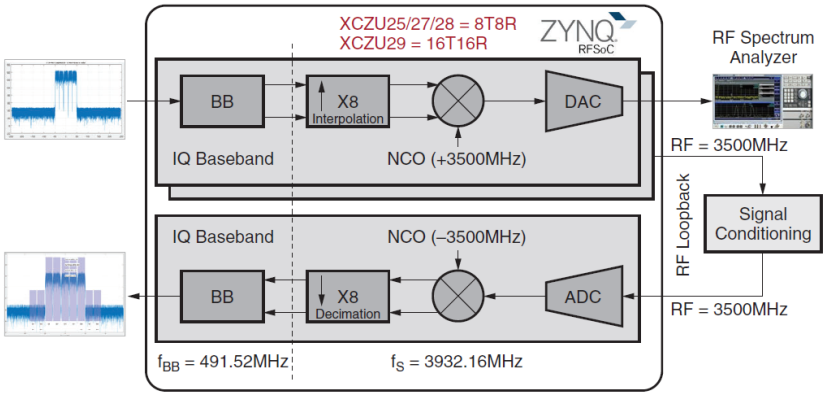

Figure 6: Adjacent channel interference measurement

converters, with the possibility to manage real and complex signals (I/Q). The structure of ADCs is based on *tiles*. Each tile is composed of 4 ADCs and 1 PLL with 12 or 14 bits operation mode. In the same way the tiles of DAC are organized with 4 14 bits DACs and 1 PLL with a bandwidth of 4 GHz and output frequency until 5 GHz. The device is 40x40-mm in size, with a 1517-pin ball grid array (BGA) package and is manufactured with a 16-nm Fin field-effect transistor (FinFET) process [15].

3.1. Processing System and Programmable logic

Like other Xilinx Zynq-based family, also RFSoC devices contain on the same chip both a processing system (PS) and programmable logic (PL). The processing system is composed of a 64-bit ARM Cortex A53 processor (1.3 GHz) used for applications and ARM Cortex R5 (533 MHz) for real-time purposes. 4 channels of PS-GTR transceivers pairs that support data rates up to 6Gb/s are also present.

The programmable logic uses CLBs with eight 6-input LUTs and 16 FFs and it is equipped with 28 Gb/s tranceivers.

3.2. Parameters Setting

Xilinx provides a graphical *RF Data Converter Evaluation Tool* that easily allows to set all data converter parameters. The GUI is shown in Figure 2 and it allows to measure some quantities such as Noise Spectral Density (NSD), third-order Intermodulation Distortion (IM3), Adjacent Channel Leakage Ratio (ACLR). The latter is measured by creating a loopback between ADC and DAC as shown in Figure 3.1.

3.3. RF Data Converters

Both ADC and DAC converters, use low-noise phase PLLs for direct clock synthesis. As introduced above, ADC tiles are organized in *tiles* containing two (4 GSps) or four converters (2 GSps), one PLL and some dedicated DSP blocks. In the tile with 4 converters, the converters are organized in pairs, and each pair can be configured separately. Figure 3.1 depicts the internal structure of ADC and DAC tile respectively.

The NSD value for DACs is usually about -160 dBm/Hz with an output carrier of 3.5 GHz. For ADCs, the value of NSD is about -153 dBm/Hz with a single input tone at 3.5 GHz. The most complex allows the use of 8 channels both for transmission and reception for a total of 16 converters with a power consumption of 9 Watt.

3.4. How to use RFSoC converters

RFSoC fully support AXI-Stream interface, that allow an high bandwidth. Furthermore, thanks to RF Data Converter tool, the user can avoid to write complex hdl controls, since a large part of the settings can be set from this GUI. Figure 3.1 shows the flow to manage RFSoC parameters and configuration.

Xilinx also provides an IP core (Zynq Ultrascale+ Zynq Data Converter) for Vivado tool. The IP core can be used for both RF-ADC and RF-DAC configuration as shown in Figure 3.4.

Also other tool companies now supports these new devices. One of the most important is Mathworks, that allow to generate HDL code of complex DSP systems including AXI-stream interface for RFSoC device (see Figure 3.4.

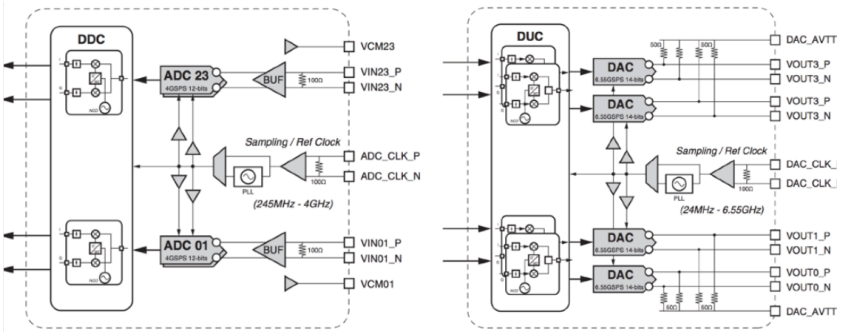

Figure 7: The Adjacent channel interference measurement

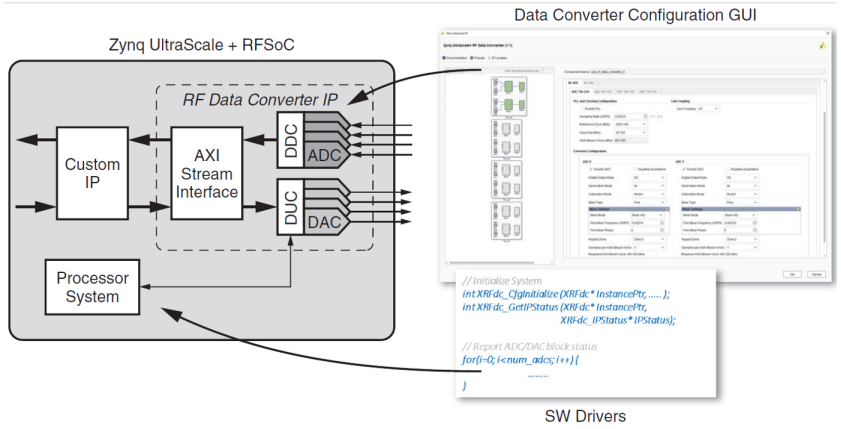

Figure 8: Platform development flow

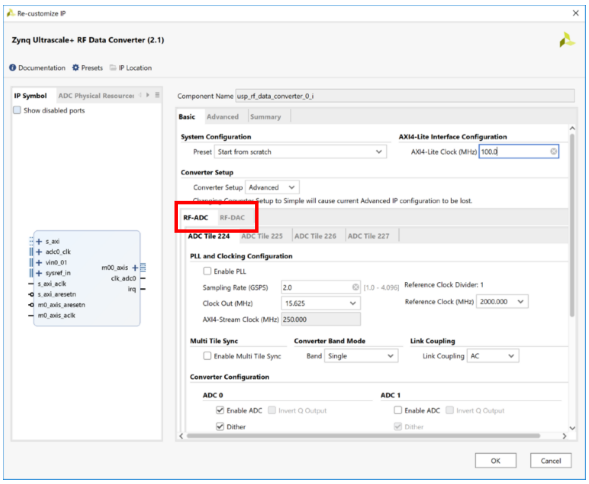

Figure 9: Vivado IP core for RFSoC

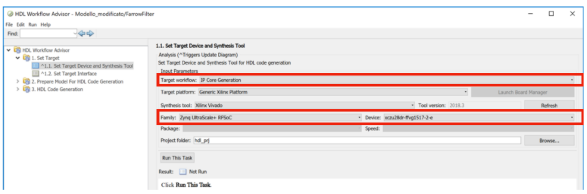

Figure 10: Matlab/Simulink HDL support for Xilinx RFSoC

4. Conclusion

In this paper, we presented the main features and potential of Xilinx RFSoCs. Thanks to RF converters (until 6 Gsps) they are very suitable for direct sampling of RF signals with bandwidth up to 4 GHz. As well as being fully supported from Vivado tool, these devices are also supported by other tools such us Mathworks Simulink.

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