Generic Approach for Structural Design Implementation and LV Automation of a Digital Block

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Abstract

As VLSI Industry uses submicron technology, Physical design and automation play a significant role to get the desired specification of design. In physical design flow along with optimum power, performance, and area there is a tradeoff between the overall turnaround time of designing. Along with it, the design must operate at the desired frequency, it must have a minimum area with good utilization and optimal power consumption. Design should be error-free and optimized before the tape-in of the design So, some automation has been done to achieve the optimum result and reduce the overall turnaround time because success depends upon the time to market and optimum performance of a design. In this paper, we have proposed a physical design Flow as well as early-stage verification with automation which can reduces the overall turnaround time.

Keywords

Structural design, Automation, Turnaround time, Power, Performance, Area

1. Introduction

As Moore's law suggests the number of transistors on a chip is going to double every two years so, These laws tend to be impractical as technology continues to advance but modern fabrication technology and design tools make it possible to industry follow Moore's law.Advancing in technology demands more functionality with as much as possible minimum chip size that leads to an increase in the complexity of the design. The physical implementation of any design is not possible without the automation tools [1] and these tools take care of the design specification and provide optimized design. The success of a product is determined by the time to market and performance. To reduce the time to market and complexity one method is to perform the early stage verification at a different stage of the physical design [2] with automation which saves too much time compared to verification [3] at the finish stage.

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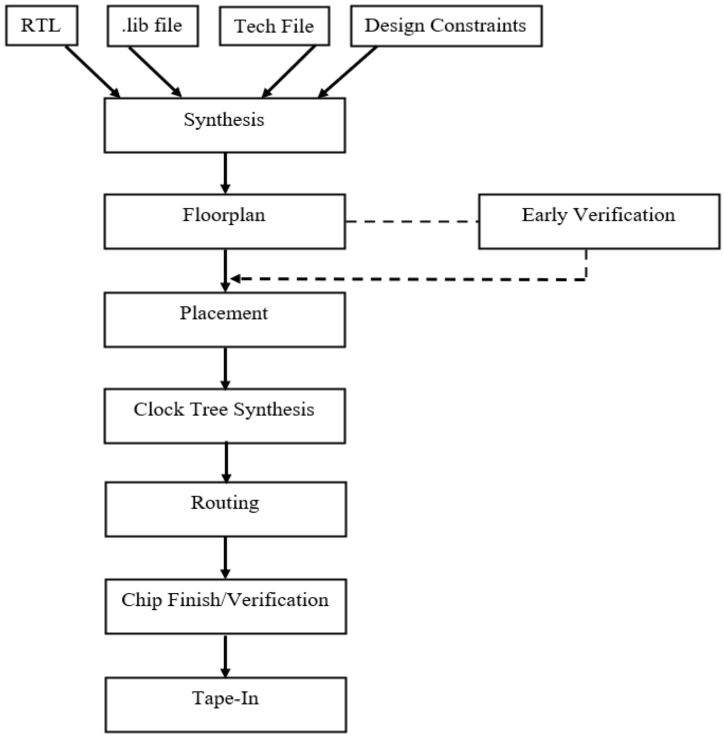

Figure 1: Physical Design Flow with Proposed Early Verification

2. Physical Design Methodology with Proposed Early Verification

Physical design [4] is a process where any idea or logic is physically implemented along with following some design rules and limitations of the fabrication process. Due to the complexity of a chip, it is divided into a small part called a block, and the process is named partition.VLSI Design Flow has two parts which are a front-end and back-end flow. There are various stages in physical design flow[2] which are shown in figure 1. During verification, it is found that there is a various violation which can be identified and rectifies at the early stage of the flow so, that we have proposed a new physical design flow with early-stage verification and done the automation which can remove the violation and save the overall time.

2.1. Synthesis

Synthesis[3] is the process of converting the RTL in the form of Gate level Netlist for targeted process technology node. We have an RTL in the form of HDL code which is converted in the form of a physical gate for a targeted technology. Synthesis [5] performs translation, optimization, and mapping on input. It has RTL, Design constraints,.lib file, tech file as input.

2.2. Floorplan

The floorplan is the art of physical design implementation because an optimized and efficient floorplan[6]causes a high-performance design architecture with optimized area utilization. Here Input is a synthesized netlist that contains the information about the standard cell, Macro, I/O pads, In the floorplan[7] first, we estimate the chip area and then placement of macros and I/O pads, tap cell, boundary cell is done, placement blockage is created. Appropriate placement of macro directly influences the timing and quality of design.

2.3. Placement

The final positioning of the logical cell in the design is done at this stage. Macro and I/O pin placement is done at the floorplan stage but other cells are left floating. Placement[8] is done in two stages global and detail placement[9]. Global placement is based on wire driven where the cell is placed based on minimum wire requirement while detail placement is timing and congestion driven so based on optimizing time and congestion placement of cell is done.

2.4. Clock Tree Synthesis (CTS)

Clock tree synthesis is the process of routing the clock network. It ensures the availability of the clock at the required point at the same time as well as lower latency and skews by adding inverter and buffer in the clock path. There are various topologies available for CTS and based on complexity we can use this topology. For the large design we use clock-mesh [6] distribution topology, it is more robust concerning variation and provides minimum skew. For small designs, H-tree is used because it is simple and easily configurable.

2.5. Routing

It is a process of connecting cells in a design with the nets. Routing[10] is done in two-stage global routing and detail routing. In global routing[11] estimation of wire length is done to route the connection path but in the detailed routing actual connection with the cell's pin using metal wire is done following global routed path. The routing can be grid-based or gridless where grids are defined by technology files that have information about the spacing between the tracks.

2.6. Chip Finish /Verification

The chip finish stage is the final step of a physical design, every performed operation is respected from a physical aspect and manufacturability perspective such as filler cells, metal filler,decap cells are added. Merging of different oasis, files take place and we get the final oasis of a design. Various verification[3] which are signoff checks like Design rule check(DRC), Electrical rule check(ERC), and LVS are performed in the oasis. After resolving all the issues, the design is completed and sent for tape-in. Tape-in is the process of generating masks and manufacturing chips.

2.7. Proposed Early Verification

It is the stage in the proposed physical design flow where we perform the verification at the early stage and designed automation to rectifies the violation.Physical design flow execution in any digital block takes number of days.Previously verification is used to perform at chip finish stage and if any violation is identified we have to switch that particular stage and rectify the violation and again rerun flow .It takes number of iterations which increases overall turn around of the product,So with the help of early verification and automation at floorplan stage we have identified the issue at floorplan stage and rectified at this stage itself which saves good amount of time that helps in minimizing the turn around time of the product.Without early verification and automation, identification of violation at chip finish stage and its rectification takes the number of iterations which increases time and complexity.

3. RESULTS

3.1. Design and Timing Report

In this paper, we have performed physical design flow in a digital block that has a different number of latches, buffers, inverters, combinational cells, macros, etc. Table 1 provides information about the design statistics.

After floorplanning and the placement macros and standard cells are placed successfully in the design. The statistics regarding area utilization of the chip have been shown in Table 2.

3.2. Automation Results

During early verification, we have found that there is a base rule violation in a design. To rectify this violation automation script has been written which automatically identifies and fixes the violation in the design as showed in figure 2 and figure 3 . There are two reasons for the base rule violation which are as follows:

- `Boundary To Tap Cell Spacing`
- `Tap To Tap Cell Misalignment`

3.3. Timing Report

There is no timing violation in the design, it is meeting setup and hold time requirement.Table 3 shows that the reg2reg path has zero setup time violation and slack.

4. CONCLUSION and FUTURE SCOPE

In this paper, we have performed the proposed physical design flow on a digital block. By using this flow and automation design is error-free along-with we can save a sufficient amount of time which helps in fast time to market of a product. Time to market is the most important factor in the industry. Early verification and automation to resolve errors at the floorplan stage, helps in minimizing time to market. In the future, we will perform early verification at

Table 1
Design Statistics

Sr.No	Name	Count
1	latchs	1896
2	Buffers/inverters	66357
3	Flip-Flop	19889
4	Macros	8
5	Standard Cells	262686

Table 2
Chip Utilization

Sr.No	Name	Utilization
1	Macro Cell Area	81326.592 um2
2	Standard Cell Area	53042.688um2
3	Chip Size	432.00 x 311.04 um2
4	Core Area	134260.416um2
5	Standard Cell Utilization	49.54

Table 3
Setup Time Violation Report

Path	WNS	TNS	Violation
Reg2Reg	0.0	0.0	0
In2Reg	0.0	0.0	0
Reg2Out	-34.98	-138.36	6
In2Out	-144.30	-1669.67	16

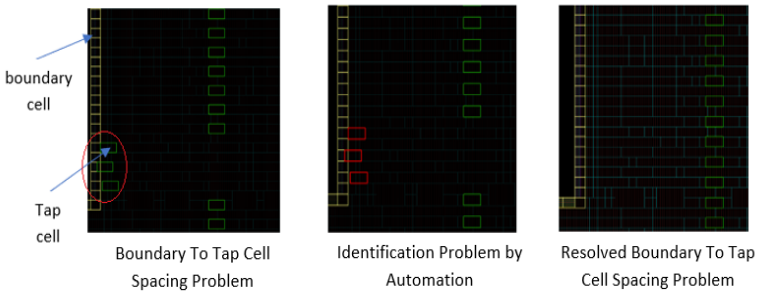
boundary cell
Tap cell
Boundary To Tap Cell Spacing Problem
Identification Problem by Automation
Resolved Boundary To Tap Cell Spacing Problem

Figure 2: Automation of boundary and tap cell Spacing Problem

placement,routing, and clock tree synthesis and develop automation, which will improve the accuracy and optimize the time to market of a product in the industry.

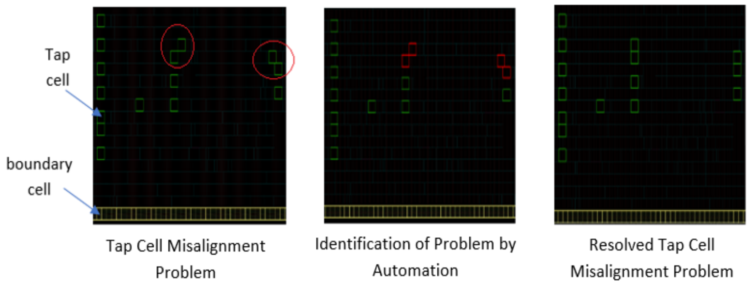
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Figure 3: Automation of boundary and tap cell Spacing Problem

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