

COMPARATIVE STUDY OF SPINTRONIC BASED STT-MRAM

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Abstract

The spintronic technology is the emerging technology specially in the industrial areas and data storage areas and the overwhelm the electronics technology. In this paper author presents the comparison with electronic technology and challenges faced by the designer while designing or fabricating the devices. The spintronic devices will cover the wide range of industrial area in upcoming years. A lot of applications are there of spintronics but here we discussed the MRAM memory because we are dealing with digital world so we need more fast, speedy, compact memory to store our data. Next the MTJ devices is also discussed which is the part of the memory and which memory is famous among all and why etc. everything is discussed in detail. Basically, this paper gives the brief introduction to the SPINTRONICS based STT-MRAM.

Keywords

Spintronics, STT, MTJ, MRAM

1. Introduction

Today, the world is almost entered into the digital world means almost everyone is working online and almost every data is stored in the devices rather than using of paper. Due to this advancement the technology also needs to be advanced with the time. The devices which are used to stored should be fast, non -volatile, use less power, small in size etc. feature is important feature in the digital world. But the existing or present CMOS technology is facing some major challenges like more power dissipation, heat dissipation, scalability limits, leakage current, etc. The device size in CMOS technology means the reduction in the gate channel length. The predictable gate length in outlook is 5nm due to this, off leakage current will be more for the complete chip[1]. But there is a limit till which we can reduce the channel length, soon engineers face other challenges like fabrication of the device, leakage current, designing, [2] etc. Through, there are numerous practices to diminish the off-chip energy and those show potentials are DG-MOSFET, Fin-FET, and Si-Nanowire MOSFET [3]. Gate MOSFET surrounded with duo material is one more method to get better carrier moving competence and trim the short cannel effect. Spin electronic is uprising, which can solve battery lifetime related problem. This increases the life of the battery by utilizing less energy from transportable gadgets to huge information centers and non-volatile features. An achievable key to overwhelm this difficulty is proposing nonvolatility in electrical circuits. Spintronic [4] gadgets are the best solution for the above-mentioned problems. [5]Spintronics or Spin logic [6] is one of the developing areas for the upcoming generation of nano-electronics devices which have absolute the Moore's law and manufacturers are struggling to go beyond law. If there is any mechanism which can compete with electronics and overcome the issues like area, power utilization and speediness etc. of the VLSI. Luckily the term called spintronic can increase the speed of device with decrease in power dissipation. To toggle on logic '0' to logic '1', the scale of the charge required to switch in the active

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region of the charge-based device due to which the current run from source to drain. It's not achievable to trim the power or heat dissipation with charge based electronic gadgets because charge only possess the direction (scalar quantity) and gives logic 1 in the presence of charge, otherwise logic 0. [7] [8] Spintronic technology basically worked on the spin property of the electron rather than the charge. In spintronic the spin moves either upward or downward or they will rotate clockwise or anticlockwise around the axis with constant frequency and represents the logic "0" or logic "1" [9]. The figure1. describes the basic working of spin.

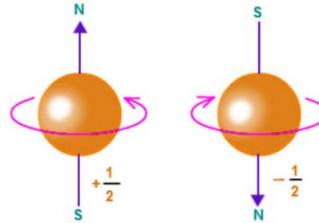


Figure 1: Spin up and spin down direction

There are various applications where the spintronic technology is used like Sensors, data storage [10], MRAM, Electrical vehicles, Magnetic sensing etc. As today's world is dealing with big data so in this paper, we focus on the spintronic memory devices i.e., MRAM [11].The comparison of the memory technology is also discussed. [12]

The paper is organized in a manner such that section 1 gives the brief introduction to the spintronics technology, section 2 describes the spintronic based MRAM, types and comparison of MRAM with other memories, section 3 gives the brief introduction to STT-MRAM, section 4 describes the operation of STT-MRAM. Finally, section 5 concludes the paper with a brief of future work.

2. MRAM (Magneto-Random Access Memory)

MRAM is the spintronic based memory [13] which provide the great advantages of small size and can easily combine with the other integrated circuits, which results in high storage speed like SRAM and high density like DRAM. Table 1 provide the comparison of different memories.

Table 1
Comparison between different memories [14][15][16].

Memory Technology	Circuit Diagram	Read Time (ns)	W/E time (ns)	Non-Volatile	Refresh	Cell Size(μm^2)	Voltage Supply(V)
SRAM		0.4	0.4	No	No	Large 0.346	1.2
DRAM		<15	<15	No	Yes 64 ms	Small 0.018	2.5
TSRAM		<3	<5	No	No	No	<0.5
Flash		14	Slow $10^3/10^2$	Yes	No	No	12/2.5
PCM		60	50/120	Yes	No	No	3
MRAM		<25	<25	Yes	No	No	1.8

The MRAM [17] can replace both the existing memories and provide great advantage. The reading data in MRAM is simple by determining the resistance of the device to fix their magnetic field. There are different approaches for writing data like Stoner-wolfarth type field switching, toggle MRAM uses Savtchenko-Switching also called as field-switching method, STT-MRAM used STT switching, and Thermally-assisted switching. The MRAM classification is done on the bases of switching methods employed to write data. The MRAM based on magnetic field is called as toggle MRAM the first generation MRAM but vanish due to difficulty in scaling the size and complex circuits and face problems when scale down beyond the limit. The next generation MRAM is STT-MRAM which can be scale down very low dimensions and can be available with plane magnetic anisotropy and Perpendicular magnetic anisotropy [18].

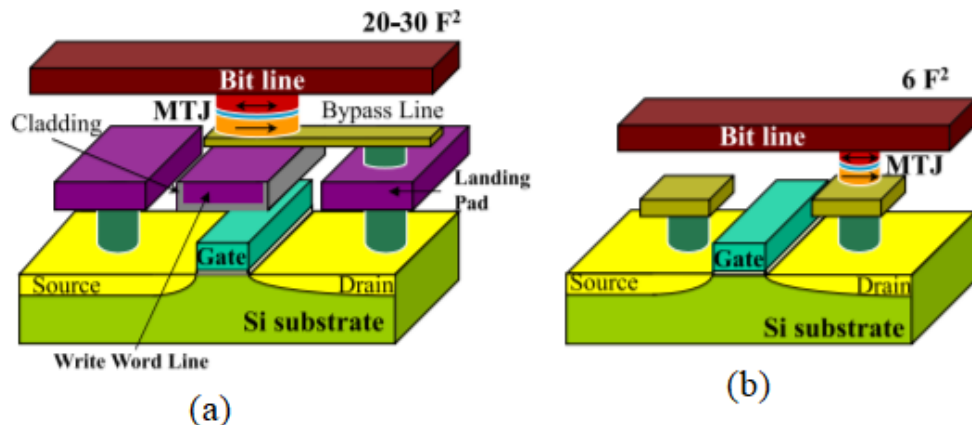


Figure 2: Structure of standard MRAM (a) and STT-MRAM (b)

The core difference among the standard MRAM and STT-MRAM [19] is that bypass line, word line and the landing pad in MRAM is removed in the STT-MRAM, hence the structure of STT-MRAM is much simpler than conventional MRAM. Moreover, the switching of STT is dependent on the current [20] density. The next third generation MRAM are also introduced like VCA, VCM, SHE, SOT. But there are some challenges which come across while using for practical implementations of MRAM circuit.

- (1) VCA straightly don't leads to predetermined shifting between dual steady states, but is used in group with one more innovation for used in an MRAM array.
- (2) For practical implementation of VCA devices, reliability issues like wear out and parameters drift need to be better understood.
- (3) SHE doesn't provide great efficiency in swapping in device with PMA.
- (4) In SOT there is need to improve the material to enhance the level of the effects for improvement in swapping efficiency.
- (5) Even in STT-MRAM there are some challenges like higher latency and energy, sensing margin is further reducing while scaling down the device and with scaling, the critical current (I_c) is leads to decrease which reduce the write energy latency. But there is a lot research is done on these challenges as mentioned in these references papers [21][22][23][24][25].

3. Introduction to MRAM (Magneto-Random Access Memory)

The basic structure of STT-MRAM consist of two parts i.e., MTJ device and the transistor [26] [27]. Further this STT-MRAM can be used as neuron and synapses in artificial intelligence and neuromorphic computing. [28] [29] [30]

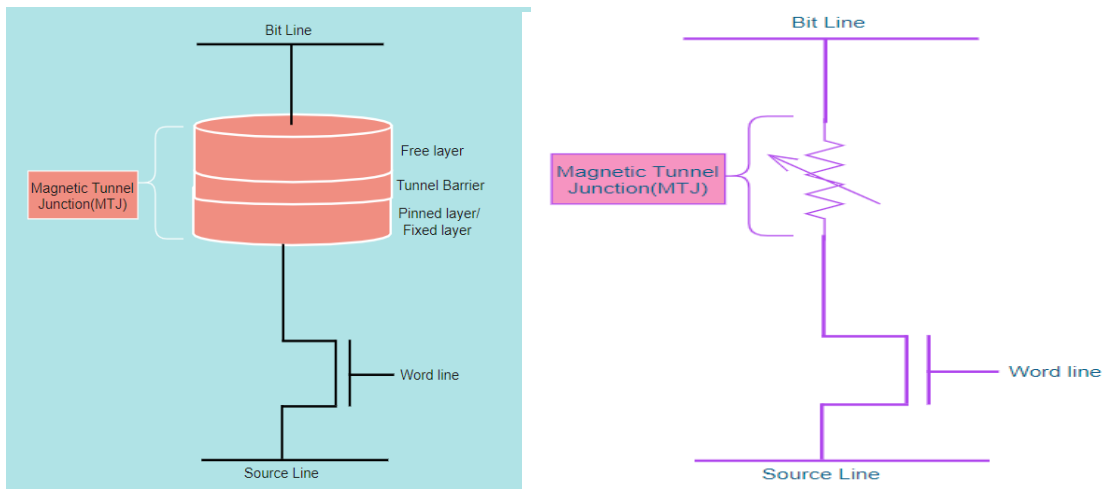


Figure3: STT-MRAM cell and Equivalent schematic

3.1. Overview OF STT (Spin Transfer Torque)

STT develop when the movement of spin angular energy in a model is not stable, except sink or sources. This occur, when the current (spin) produced from the spin filtering method via passing it through one magnetic slim film of different moment and the same current is strained by the other magnetic slim film with different moment. Because the moment of both layers is not collinear with each other so some part of the spin angular energy which is hold by the electron's spin is taken by the second magnet film. Moreover, when spin polarized electrons exceed over the magnetic-domain wall or some space based unequal magnetization dispersion. In this cycle, the charge of the spin electron revolves to track the native magnetic area and because of this angular energy spin vector movement vary as a function of position. In both situations the magnetic field of the metal (Ferro-magnet) transform the movement of spin angular energy by applying the torque on the moving spin to redirect them and as result the moving electron apply the same and reverse torque on the metal. Now this torque which is enforced by imbalance of electron conduction on metal is termed as spin transfer torque.

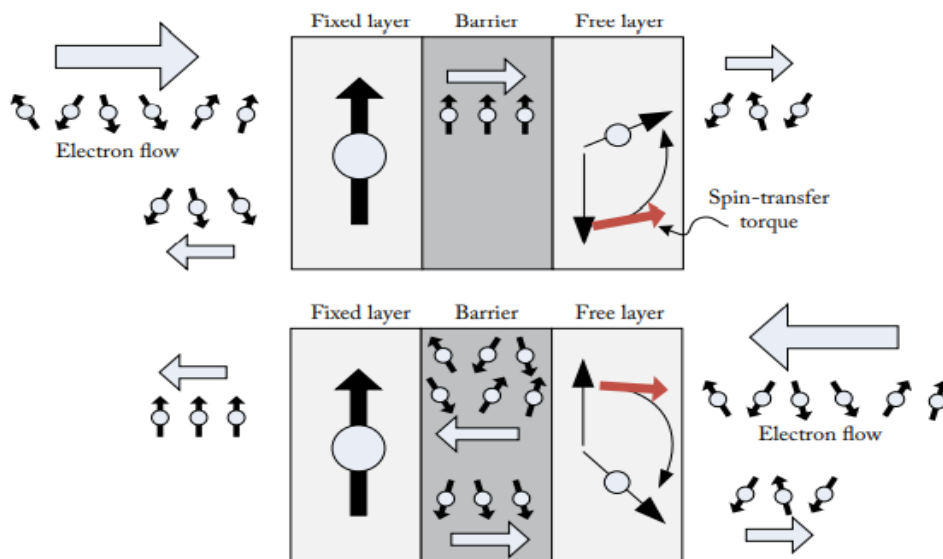


Figure4: STT effect

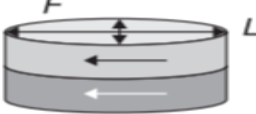
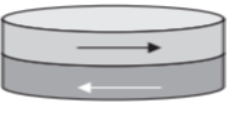

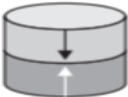
The intensity of torque can be estimated in two ways that is by directly considering the common precession of the spin and magnetic significance during the time of interaction or by taking the complete variation in the spin's current before and after the interaction. [31]

3.2. Introduction to MTJ (Magnetic Tunnel Junction)

The MTJ [32] is the heart of the STT-MRAM. The MTJ device is used to store the data of the STT-MRAM. According to the direction of the magnetic easy axis of the magnetic layers of MTJ, the MTJ is divided into two types. A magnetic easy axis is the direction in which magnetization assumes the lowest energy. The types are: (a) in-plane-MTJ; (b) Perpendicular-MTJ. The table I shows the parallel and antiparallel state of MTJ type. The MTJ consist of three different layers in which two layers are of ferromagnetic layers divided by the thin insulator layer (nonconducting Tunnel barrier). The free layer is composed of metals like Fe, Co and Ni and their alloys. The fixed layer and the pinned layer are coupled anti ferromagnetically over Ru-layer to create SAF (Synthetic Anti Ferro Magnet). In i-MTJ, due to high switching current density it is not compatible with CMOS technology so p-MTJ is used. [33]

Table 2

MTJ types with its state

MTJ type	Aspect ratio $k = L/F$	Parallel	Antiparallel
In-plane anisotropy MTJ (i-MTJ)	> 1		
Perpendicular anisotropy MTJ (p-MTJ)	1		

One layer is the thicker layer because it contains some layered(stack) structure with its fixed magnetic alignment called as fixed layer or pinned layer (PL) and other layer is thinner one whose magnetization is not fixed and varied as per applied external magnetic field [34] . The device displays two resistive conditions which depend upon the relative alignment of orientation direction of two ferromagnetic layers due to the spin-dependent tunneling involved in the electrons transport among the majority and minority spin states. In parallel state, the MTJ offer low resistance because both the layers i.e., free layer (FL) and pinned layer are magnetized in the same direction whereas when the direction of magnetization of both layer is antiparallel it offers high resistance [35].with this high and low resistance of MTJ '0' or '1' can be stored. Change in the resistance is calculated using the TMR (Tunnel Magnetoresistance) ratio. The TMR ratio should be high is the main parameter of the memory and logic applications and the ratio reaches at 500% at room temperature when oxide barrier is composed of MgO.

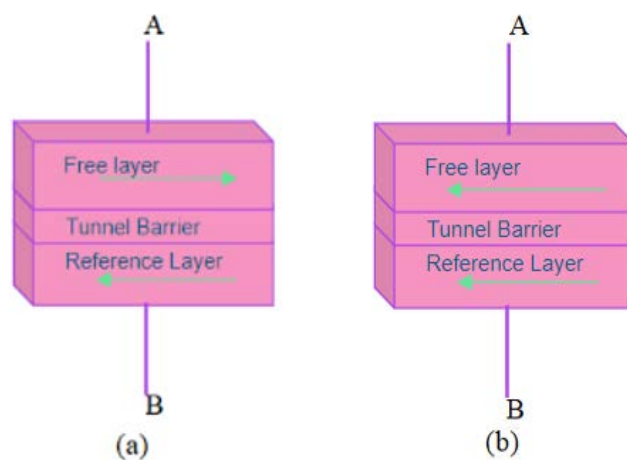


Figure5: MTJ states (a) Anti-parallel (high-resistance) (b) Parallel (low-resistance)

3.3. Properties of the Spin Transfer Torque-MTJ

3.3.1. TMR(Tunnel Magneto-Resistance)

The MTJs shows a great variation between parallel (R_p) and anti-parallel (R_{ap})resistance and reason behind this difference is coherent tunneling[36]. The term TMR is defined as the ratio of above-mentioned resistances and represented in eq. (1).[37]

$$TMR = \frac{R_{ap} - R_p}{R_p} \quad (1)$$

When there is change in bias voltage(v), the TMR ration also vary. When bias voltage is increasing the parallel resistance decrease, which is also not symmetric for positive a negative bias voltage and it remain unchanged in case of anti-parallel state.

3.3.2. Critical Switching Current

Another important property of MTJ is critical switching current and explain in which condition did MTJ will stay either parallel or anti -parallel. It is termed as the function of switching time (τ) and operating temperature(T) and represented in equation (2) [38]□

$$I_c = I_{co} \left\{ 1 - \left(\frac{KT}{E} \right) \ln \left(\frac{\tau}{\tau_0} \right) \right\} \quad (2)$$

The workstation simulations play vital task in designing the circuits and precision of the simulation results rely upon how correct device models were used in simulations. The main focus is to design the suitable MTJ for latest PTM models or technology. There was a lot of research done on the designing of MTJ with micromodel's, using Verilog codes or circuit implementation using LLG equation etc. but there were many challenges like in some papers the results were not matched, somewhere complex equations were used to design the MTJ models [39][40][41][42][43][44]

4. Operation of STT based MRAM

The cell organization of Spin Transfer Torque based MRAM is explained above which consists of 1T1MTJ i.e., a transistor and one MTJ devices. The storing process of data in MTJ device is guarded by wordline at transistor. During the writing process, the input is applied among bit line and source line so that the switching current can rush along MTJ. Relying upon the voltage polarity '0' or '1' can be written. Let's illustrate that MTJ captivation will be in parallel thru fixed layer when the current flow from the bitline to source line then and '0' is written into the cell. while reading the info from the memory cell the sensing input voltage is applied among the source and bit line, and the current rush along the MTJ's is evaluated with the current flowing over the reference cell. The dissimilarity between the sensing current will tell the what data is stored in cell. Meanwhile the difference of the current is extremely less, so sense amplifier is used to amplify it, then this amplified signal is applied to upcoming circuit.

5. Conclusion

This paper presents the overview of the spintronics STT-MRAM which is best suited memory for storing data with simple and easy circuit only consist of two components. The comparison with other memories is also discussed which give idea that what features matter in the memory. Next the STT-MRAM is better than other generation memories are also discussed. Moreover, the different modeling techniques are also mention that how MTJ device can be created in the software by using different methods. The main aim of the author is to explain you the basis of STT-MRAM and why this MRAM is famous among all memories. The MTJ is the main device which is based on the spintronic technology and store and read data in 0 and 1. The MTJ can be designed by using different approaches and software. The best way to design the MTJ is by using Verilog-A code because the circuit of MTJ consist of many complex circuits based on resistance and capacitors. The main focus

of the author is to describe the spintronic based memory with other CMOS based memories. For future work one can design the memory with lowest technology of CMOS as the MTJ can be scaled to lowest nodes and scalability of MTJ is easier. Further the memory designed with lowest technology can be used to design neuron or synaptic when used in Artificial intelligence and neuromorphic computing.

6. References

- [1] "The International Technology Roadmap for Semiconductors published by the semiconductor Industry Association," [Online]. Available: <<http://www.itrs.net>>..
- [2] Shivani Chopra , Subha Subramaniam, "A Review on Challenges for MOSFET Scaling," *IJISET - International Journal of Innovative Science, Engineering & Technology*, vol. 2, no. 4, pp. 1055-1057, April 2015.
- [3] S Singh, B Raj, "Design and analysis of hetrojunction Vertical T-shaped Tunnel Field Effect Transistor", *Journal of Electronics Material*, Springer, Volume 48, Issue 10, pp 6253–6260, October 2019.
- [4] Hirohota. A. et al., "Review on spintronics: Principle and devices applications," *J ournal of Magnetism and Magnetic Materials*, vol. 509, pp. 166711-39, March 2020.
- [5] Prof Manilal D Amipara, ""Nano Technology - Spintronics"," *IOSR Journal of Electronics and communication Engineering (IOSR-JECE)*, pp. 14-18, 2014.
- [6] C Goyal, J S Ubhi and B Raj, "A Low Leakage CNTFET based Inexact Full Adder for Low Power Image Processing Applications", *International Journal of Circuit Theory and Applications*, Wiley, Volume47, Issue9, Pages 1446-1458, September 2019.
- [7] Abhishek Gautam, "Spintronic- A new hope for the digital world," *International Journal of Scientific and Research Publications*, vol. 2, no. 8, pp. 1-5, August 2012.
- [8] Sharma, S. K., Raj, B., Khosla, M., "Enhanced Photosensitivity of Highly Spectrum Selective Cylindrical Gate In_{1-x}GaxAs Nanowire MOSFET Photodetector, *Modern Physics letter-B*, Vol. 33, No. 12, PP. 1950144 (2019).
- [9] Albert Fert , " "The origin, development and prospects of spintronics," ,, " *Physics usp.*, vol. 51, no. 1336, pp. 1-11, 2008..
- [10] Yu, S. and Chen, P. Y., " "Emerging memory technologies: recent trends and prospects," " *IEEE Solid-State Circuits Mag.* , vol. 8, no. 2, p. 43–56, 2016.
- [11] J Singh, B Raj, "Design and Investigation of 7T2M NVSARM with Enhanced Stability and Temperature Impact on Store/Restore Energy", *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 27, Issure 6, PP. 1322 - 1328 June 2019.
- [12] Endoh, T. and Honjo, H., "A recent progress of spintronics devices for integrated circuit applications," *J. Low Power Electron. Appl.*, vol. 8, no. 4, 2018.
- [13] A K Bhardwaj, S Gupta, B Raj, Amandeep Singh, "Impact of Double Gate Geometry on the Performance of Carbon Nanotube Field Effect Transistor Structures for Low Power Digital Design", *Computational and Theoretical Nanoscience*, ASP, Vol. 16, PP. 1813–1820, 2019.
- [14] Wong, H.S.P., Raoux, S., Kim, S., Liang, J., Reifenberg, J.P., Rajendran, B., Asheghi, M. and Goodson, K.E., ""Phase change memory," " *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2201-2227 , 2010.
- [15] C Goyal, J SUBhi and B Raj, Low Leakage Zero Ground Noise Nanoscale Full Adder using Source Biasing Technique, "Journal of Nanoelectronics and Optoelectronics", American Scientific Publishers, Vol. 14, PP. 360–370, March 2019.
- [16] Kawahara, T., Ito, K., Takemura, R. and Ohno, H., " "Spin-transfer torque RAM technology: review and prospect," " *Microelectron. Reliab.* , vol. 52, no. 4, pp. 613-627, 2012.

- [17] Kang, W., Ran, Y., Zhang, Y., Lv, W. and Zhao, W., "Modeling and exploration of the voltage-controlled magnetic anisotropy effect for the next-generation low-power and high-speed MRAM applications," *IEEE Trans. Nanotechnology*, vol. 16, no. 3, p. 387–395, 2017.
- [18] A Singh, M Khosla, B Raj, "Design and Analysis of Dynamically Configurable Electrostatic Doped Carbon Nanotube Tunnel FET," *Microelectronics Journal, Elsevier, Volume 85*, Pages 17-24, March 2019.
- [19] Apalkov et al., "Magnetoresistive Random Access Memory," *Proceedings of the IEEE*, vol. 104, no. 10, pp. 1796-1830, 2016.
- [20] C Goyal, J S Ubhi and B Raj, A reliable leakage reduction technique for approximate full adder with reduced ground bounce noise, *Journal of Mathematical Problems in Engineering, Hindawi, Volume 2018, Article ID 3501041*, 16 pages, 15 Oct 2018.
- [21] D. Zhang et al., "High-Speed, Low-Power, and Error-Free Asynchronous Write Circuit for STT-MRAM and Logic," *IEEE Transactions on Magnetics*, vol. 52, no. 8, pp. 1-4, August 2016.
- [22] G Wadhwa, B Raj, "Label Free Detection of Biomolecules using Charge-Plasma-Based Gate Underlap Dielectric Modulated Junctionless TFET" *Journal of Electronic Materials (JEMS)*, Springer, Volume 47, Issue 8, pp 4683–4693, August 2018.
- [23] E. Kültürsay, M. Kandemir, A. Sivasubramaniam and O. Mutlu, "Evaluating STT-RAM as an energy-efficient main memory alternative," *2013 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp. 256-267, 2013.
- [24] G Wadhwa, B Raj, "Parametric Variation Analysis of Charge-Plasma-based Dielectric Modulated JLTFET for Biosensor Application" *IEEE Sensor Journal*, VOL. 18, NO. 15, AUGUST 1, 2018 .
- [25] Im and S. Park., "A Read–Write Circuit for STT-MRAM With Stochastic Switchings," *in IEEE Transactions on Magnetics*, vol. 54, no. 5, pp. 1-7, May 2018.
- [26] D Yadav, S S Chouhan, S K Vishvakarma and B Raj, " Application Specific Microcontroller Design for IoT based WSN", *Sensor Letter, ASP, Vol. 16, PP. 374–385*, May 2018.
- [27] G Singh, R. K. Sarin and B Raj, "Fault-Tolerant Design and Analysis of Quantum-Dot Cellular Automata Based Circuits", *IEEE/IET Circuits, Devices & Systems*, Vol. 12, PP. 638 – 64, 2018.
- [28] A. Senugupta and K. Roy , ""Spin-Transfer torque Magnetic neuron for low power neuromorphic computing"," *International joint conference on Neural Networks(IJCNN)*, pp. 1-7, 2015.
- [29] S.R.Kulkarni ,D.V.Kadetotad,S.Yin, J Seo and B.Rajendran, ""Neuromorphic Hardware Accelerator for SNN interface based on STT-RAM crossbar arrays."," *26th IEEE International conferences on Electronics, Circuits and system (ICECS)*, pp. 438-441, January 2020.
- [30] Binpin Rajendran,Fabien Alibart, "Neuromorphic computing based on emerging memory technologies.," *IEEE Journal on emerging and selected topics in circuits and systems* , vol. 6, no. 2, pp. 198-211, 2016.
- [31] D.C. Ralph, M.D. Stiles, "Spin transfer torque," vol. 320, no. 7, pp. 1190-1216, April 2008.
- [32] H.J.M. Swagten, P.V. Paluskar, "Magnetic Tunnel Junctions," *Encyclopedia of Materials: Science and Technology*, pp. 1-7, 2010.
- [33] W Bi et al. , "An architecture-level cache simulation framework supporting advanced PMA STT-MRAM," *NANOARCH:Nanoscale architectures*, pp. 7-12, June 2015.
- [34] Cobas, Enrique, et al., " "Graphene-based magnetictunnel junctions".,," *IEEE Transactions on Magnetics*, vol. 49, no. 7, pp. 4343-4346, 2013..
- [35] Mahmoudi, Hiwa, Thomas Windbacher, Viktor, ""Design and applications of magnetic tunnel junction based logic circuit," *IEEE Conference on Ph. D. Research in*

Microelectronics and Electronics (PRIME), pp. 157-160, 2013.

- [36] J Singh, B Raj, "Modeling of Mean Barrier Height Levying Various Image Forces of Metal Insulator Metal Structure to Enhance the Performance of Conductive Filament Based Memristor Model", *IEEE Nanotechnology*, Vol. 17, No. 2, PP. 268-267, March 2018.
- [37] J.Z. Sun, D.C. Ralph, "'Magnetoresistance and spin-transfer torque in magnetic tunnel junctions,'" *Journal of Magnetism and Magnetic Materials* ,, pp. 1227-1237, 2008.
- [38] A Jain, S Sharma, B Raj, "Analysis of Triple Metal Surrounding Gate (TM-SG) III-V Nanowire MOSFET for Photosensing Application", *Opto-electronics Journal*, Elsevier, Volume 26, Issue 2, Pages 141-148, May 2018.
- [39] W. Zhao, E. Belhaire, Q. Mistral, C. Chapped, V. Javerliac, B.Dieny, E. Nicolle, "Macro-model of Spin-Transfer Torquebased Magnetic Tunnel Junction device for hybrid Magnetic-CMOS design," *IEEE, Proceedings of Behavioral Modeling and Simulation Workshop*, pp. 40-43, 2006.
- [40] N Jain, B Raj, "Parasitic Capacitance and Resistance Model Development and Optimization of Raised Source/Drain SOI FinFET Structure for Analog Circuit Applications, *Journal of Nanoelectronics and Optoelectronins*, ASP, USA, Vol. 13, PP. 531–539, Apl 2018 .
- [41] Jonathan D. Harms, Farbod Ebrahimi, Xiaofeng Yao, Jian Ping Wang, "SPICE macromodel of spin-torque-transfer-operated magnetic tunnel junctions," *IEEE Transactions on Electron Devices*,, vol. 57, no. 6, pp. 1425-1430, 2010.
- [42] Seungyeon Lee ,Hyunjoo Lee ,Sojeong Kim ,Seungjun Lee,Hyungsoon Shin, "A novel macro-model for spin-transfer-torque based magnetic-tunnel-junction elements," *Solid-State Electronics*,, vol. 54, no. 4, pp. 497-503, 2010.
- [43] Rishubh Garg, Jyoti Kedia, " A novel verilog-A model of spin Torque Transfer Magnetic Tunnel Junction," *Universal journals of physics and application* , vol. 1, no. 3, pp. 290-294, 2013.
- [44] Yue Zhang et al. , "Compact modeling of perpendicular -anisotropy CoFeB/MgO Magentic tunnel junction," *IEEE transactions on electron devices*, vol. 59, no. 3, pp. 819-825, March 21012.