Comparative Analysis of Multiplications Technique Using Vedic Mathematics

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Abstract

Vedic mathematics influenced from the ancient arithmetic system of the Vedas makes the regular mathematical calculation at more ease as it can be done by mental approaches. In This paper we are going to presents the concepts and theories behind the Urdhva Tiryagbhyam and Nikhilam Sutra. In this paper, the designs of 4 X4 bits Urdhva Tiryagbhyam, Nikhilam Sutra on kit Spartan 3 XC3S50-5-PQ- 208 have been used. The calculated delay regarding computation for 4X4 Urdhva Tiryagbhyam was 14.14 ns and power is 20.60 mw for Nikhilam Sutra the calculated computational delay is 16.16 ns and total power consumption is 24.60 mw.

Keywords

Vedic mathematics, algorithm, UT, MAC, CIAF, DSP, FFT

1. Introduction

The experience of the Multiply and Accumulate (MAC) is the basis for multiplication and in-house products at some of the common computationally intensive Counting Functions (CIAF), which have been used and are currently being used by a lot of Digital signal Processing (DSP) applications, that is, of course, the secret of correspondence, filtration, and industrial applications, in its arithmetic and logic unit, the fast Fourier transform (FFT). This is a must-have for a fast multiplier, since the multiplication is dominated by the time to perform the majority of the DSP algorithms. In order for a certain period of time, the SOUND team, chips, multiplication time is still the most important factor. As a result of the use of the software and processing software, the need for high-speed processing has been increasing. The application of the same type are to be achieved on the basis of the high pass rate of the aerometric activity .One of the significant arithmetic operations such as multiplication and progress, and the rapidmultiplication systems has been an area of interest in the last few decades. Many of the programs in order to reduce the delay and power consumption are very essential requirements. In a digital circuit design, as it is most commonly used ingredients is the digital opinion leaders. They are used to carry out a transaction, such as they are, is the fastest, most reliable, and most efficient components. Today, many of the algorithms of features, multiplication, and each one offers different benefits and trade-offs in terms of energy, speed, circuit complexity, and in the field. The most important components in many digital signal processors (DSP), it is called a digital multiplier, and the rate of their multipliers is determined by the speed of the DSP. Thematrix multiplication algorithm and a Box, the multiplication algorithms are two of the most commonly used property of multiplication algorithms, which are used in the field of digital computer hardware. For the moment, to carry out the calculations with the use of the array multiplier is relatively small, since these are calculated, regardless of their parallel ones. The amount of time that it takes to multiply by

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the front door is visible from the windows of the multiplication of series, which is called the grip. For high-speed multiplication, the use of large booth, chains, and a big one at that, is registered for a certain amount, and the relocation will require an exponentialoperation. In this article, we are going to discuss about two methods that Nikhilam Sutra Urdhva tiryagbhyam (at output), the binary number system has got itself first applied with the sutras and the system is used for the development of the different digital devices.

1.1 Need for Vedic mathematics

1. It lessens the scratch from finger.
2. It consumes the less time.
3. An influential tool regarding calculation.
4. Solution is presented in a single line.
5. Better work force.

1.2 Applications of multiplier

Multipliers are widely used in

1. For convolutions, factorial calculations.
2. Arithmetic and logic unit in processors
3. For various mathematical operationslike rooting, Divisions
4. Floating point units
5. FIR filters
6. Speech synthesis/recognition
7. DSP algorithms such as FFT DFT
8. Math processor
9. In cryptography

2. Vedic multiplication Algorithms

The Vedic multiplier focused in this work is leaned on the formula of Vedic multiplication which are sutras. The sutras find their usage in the decimal number multiplication.

2.1. Urdhva Tiryagbhyam sutra

Urdhva Tiryagbhyam multiplier is actually an algorithm of Vedic mathematicsdiscovered in India during the Vedic era. If we tell about the sutras, it is a formula and related to multiplier mainly “vertical and crosswise” .Here the partial product generatedand concluded with the partial product of concurrent addition

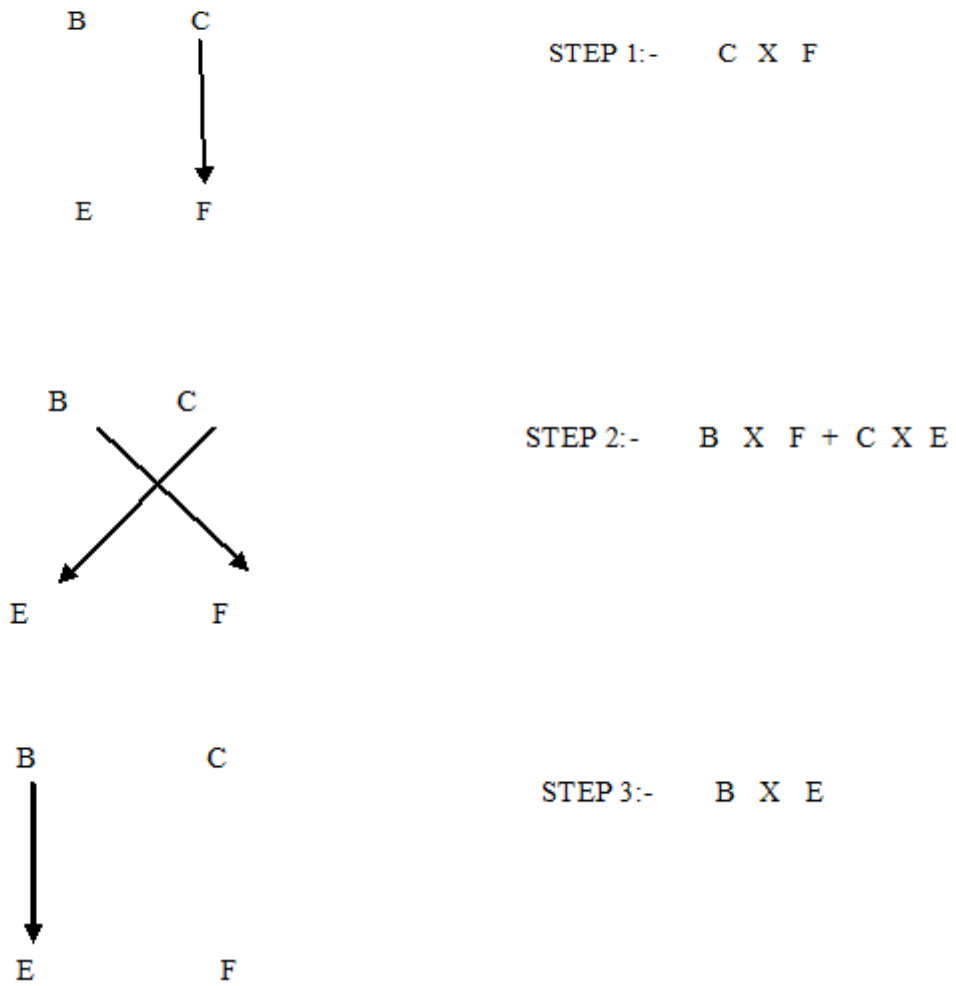

Figure 1: General formula for Vedic multiplications

Example

$$\begin{array}{r} 46 \\ \times\ 43 \\ \hline 1978 \end{array}$$

2.2. Nikhliam sutra

Multiplication for the base 10 numbers are performed by Nikhliam Sutra (e.g.: 97 x 94 or 103 x 105).

Sample (i):- Numbers (2 no) < Base.

$$\begin{array}{rrr} & 97 & 3 \\ \times & 94 & 6 \\ \hline & 9118 & \end{array}$$

Sample (ii):- Numbers (2 no) > Base.

104 4

X 105 5

1 0, 9 2 0

Sample (iii):- One number lower and other one higher than the base.

103 3

X 98 -2

1 0, 0 9 4

3. Simulations and results

The Urdwa Sutra, Nikhliam Sutra can be implementing on the Xilinx 8.1 and family used SPARTAN 3 and device XC3S50E the synthesis report for HDL is shown in Table 1. The output waveform of 4x4 urdhwa sutra is shown in Figure 2. In this case apply data in the form of bits and output is displayed at the end of y (output). The output waveform of 4x4 nikhilam sutra is shown in Figure 3. In this case apply data in the form of bits and output is displayed at the end of y (output).

Table 1
HDL Synthesis Report

Device Spartan 3XC3S50-5-PQ-208	4x4 Urdwa Sutra	4x4 NIKHLIAM SUTRA
Delay	14.14ns	16.16ns
Power consumptions	20.60mw	24.62mw
Number of slices	23 out of 768 (2%)	16 out of 2448 (1%)
Number of inputs LUT	40 out of 1536 (2 %)	29 out of 4896 (1%)
Number of bonded IOBs	17 out of 146 (11%)	16 out of 152 (10%)

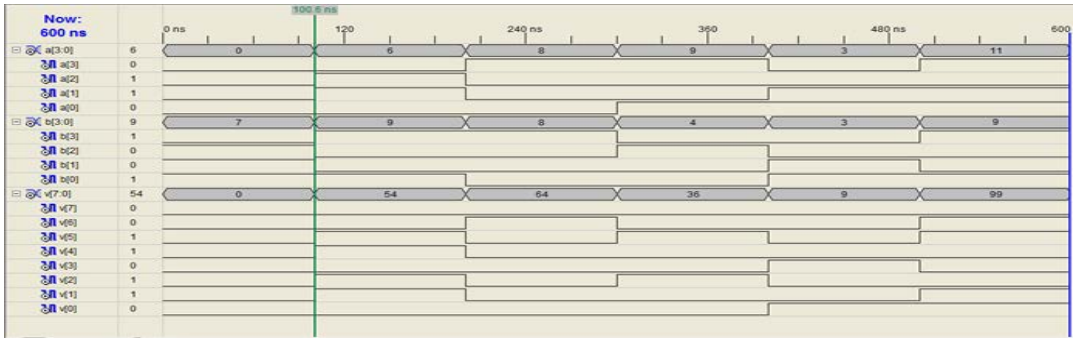

Figure 2: Waveform for 4 x 4 urdhva sutra

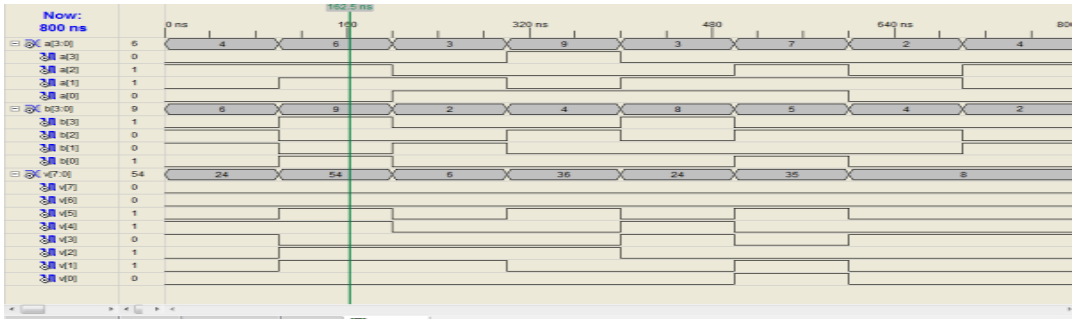

Figure 3: Waveform for Nikhilam sutra

4. Conclusions

The designs of 4 X4 bits Urdhva Tiryagbhyam, Nikhilam Sutra have been implemented on Spartan XC2S50E-5-PQ-208. The computation delay for 4X4 Urdhva Tiryagbhyam was 14.14 ns and power is 20.60 mw. For Nikhilam Sutra the computational delay is 16.16 ns and power consumption is 24.60 mw. So from above results the Urdhva Tiryagbhyam has best sutra because it occupies the less delay and power consumptions.

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