Comparing 6T & 13T SRAM Bit Cell & using FinFET to construct the superior in 22nm Scale for usage in Spacecrafts

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Abstract

The soft error in SRAM is generated as the single ionizing particle strikes a sensitive node ,which gives rise to Single Event Upsets (SEU)[1] .Here in this paper we design and examine the 6T and 13T SRAMs and use FinFET[2,3] in 22nm technology node in Cadence Virtuoso and Tanner EDA Tool . A feedback which would be driven on dual mode would be added to the design, to combat the residual deposition of charges

Keywords

FinFET , SEU and SRAM

1. Introduction

The future space communication depends on the merging the VLSI chips with the satellites or any other application in space technology . The major challenge will arise when the radiation problem will come into play as the circuits are fed with supply voltages .The most needed for the future are the Ultra Low Power devices which can be achieved by using satellites having a significantly low supply voltage , which means lesser threshold and sub threshold voltage . For every devices the weight of the batteries does matter same as for the satellites . When light weight satellites are needed the batteries with low supply voltages can be made , now as the technologies are scaled down and these reduced dimensions leads to an increment in the complexity , which in turn leads to the generation of the short channel effects and there is a threat for the damage in the device due to the leakage issues. The devices which are resistant to low voltage faults must be having two most important aspects . Firstly they must be (ULP) [1] or Ultra low Power consumption devices and also must be guarded against soft errors . The soft errors can be controlled by Error Correction Coding . Now in order for better control of the devices we move ahead from the normal CMOS technology to bit lower technology nodes .From here the FinFET comes into the picture .FinFET is such a device with a control of gate all round from proper leakage current control .This would lead to low power consumption devices and smaller processor size .Better robustness of the circuits manufactures and our target of ULP or the ultra low power consumption device can be achieved. The domination over the normal Planar FET can be taken over by FinFETs[2,3] with better scalability, better control of power consumption , proper control of short channel effects . Here we would be using 22nm technology node which is very much favourable for significant performance , better control of devices to weight of devices and even low power consumption.

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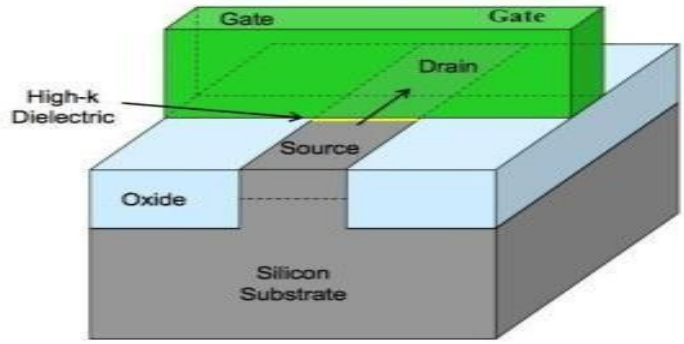

Figure 1: Cross Section view of FinFET with Gate All Around Structure.

1.1 SEU Effect on 6T SRAM

The SRAM bit cell is a kind of latch used to store one bit of information. The SRAM bit cell is a part of the array in the memory . The SRAM bit cell is having to back to back NOT gates connected in a crossover position . The SRAM if presented in CMOS design , one bit cell will be storing 1 bit of information and represented by PMOS and NMOS gates by two inverter circuits.The bit lines and the write lines would be responsible for the read and write operations respectively. The three modes of operations are the READ,WRITE & HOLD. The access transistors will have to be isolated from the supply for the HOLD operation.

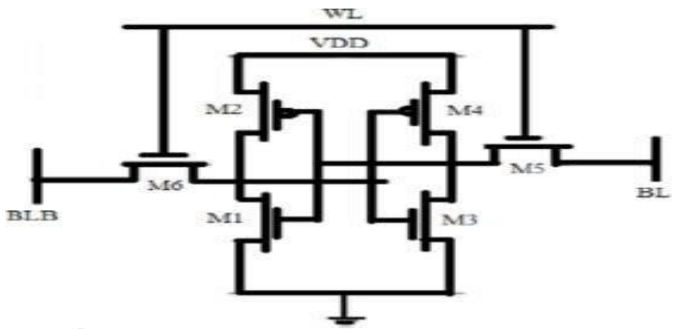

Figure 2: Circuit for 6T SRAM 1 Bit cell.

The sensitivity of the 6T SRAM memory cell circuit is prone to soft errors like Single Event Upset[4]. The SEU may not permanently disrupt the circuit by may cause error when the circuit will be working under low voltage supply and the sub threshold voltage will decrease . This will result to a change in the bit and the SEU exposure of the circuit will increase which in turn will boost its sensitivity to the soft errors.

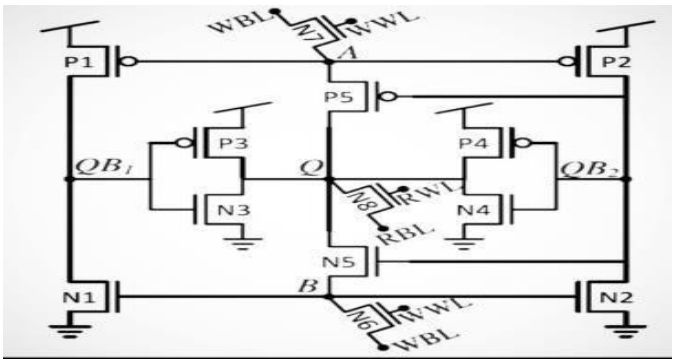

Figure 3: Circuit for FinFET based SRAM cell with 13T.

The circuit proposed above in Fig: 3 is the structure of 13T SRAM bit cell with feedback mechanism which is dually driven. This structure in all the way is very much robust , low voltage circuit which would be supporting ultra low power mechanism for space technology . Therefore we can say that these can be a significant contribution for light weight satellites . As shown in Fig 3 the 13T SRAM bit cell are having five different nodes for storage purposes from QB1 to QB2 and then to Q which would act as a storage node . As for driving we would be having the two crossover inverters . A dually driven mechanism with feedback is given for protection from soft errors like Single Event Upset.

2. Results and Discussion

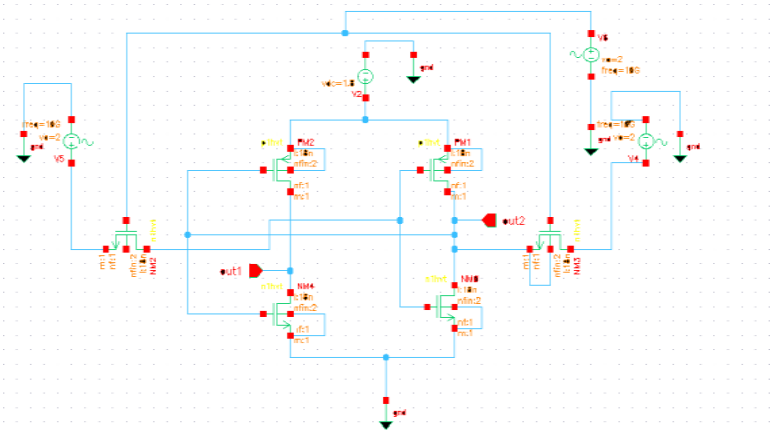

Figure 4: READ MODE for a 6T based SRAM memory cell.

In HOLD the word line is low (WL = GND), so that access transistors will be LOW (M5 and M6) and there won't be any data pushed into bits of any of the cells. The cross coupled mode of the inverters will have their feedback activated and when there will be proper supply the latch will lead to holding of the data.

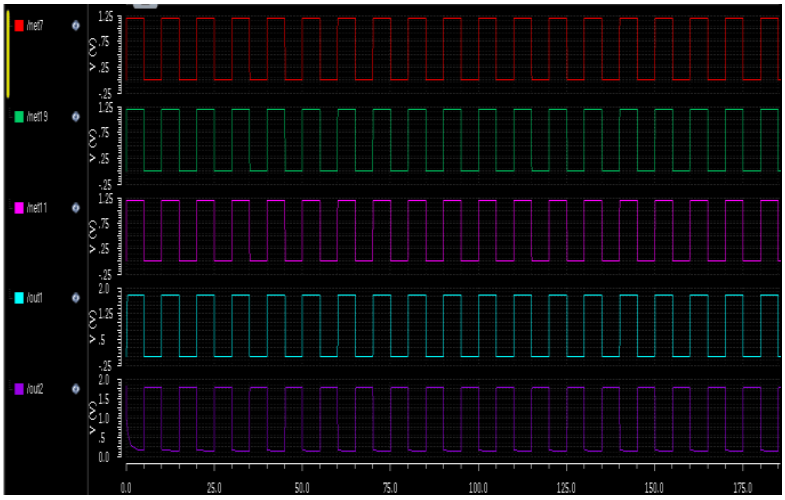

Figure 5 : Simulation output for operation of 6T SRAM bit cell.

The 6T SRAM's major failure is when the pull down transistor is very much weaker than the access transistor[4,5]. This leads to the read failures ; this major issue is taken care of the the 13T SRAM bit cells where the transistor pair of N3 and N4 is added. The Q output will have a stable value for feedback mode which is dually driven. The output of the proposed model of 13T SRAM bit cell is given in Fig:7 & Fig:8 , along with all the modes of operation.

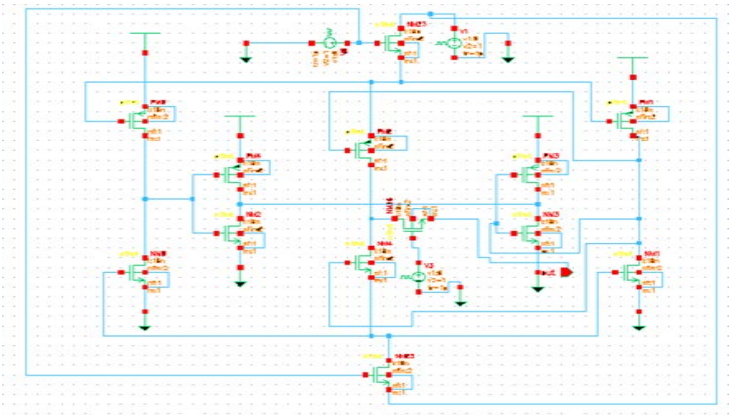

Figure 6 : Proposed structure for 13T SRAM memory bit- cell schematic diagram .

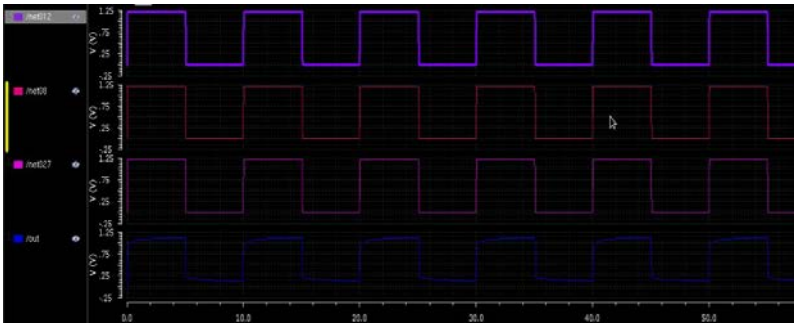

Figure 7 : Simulated waveform for Logic 0 condition for 13 T SRAM cell.

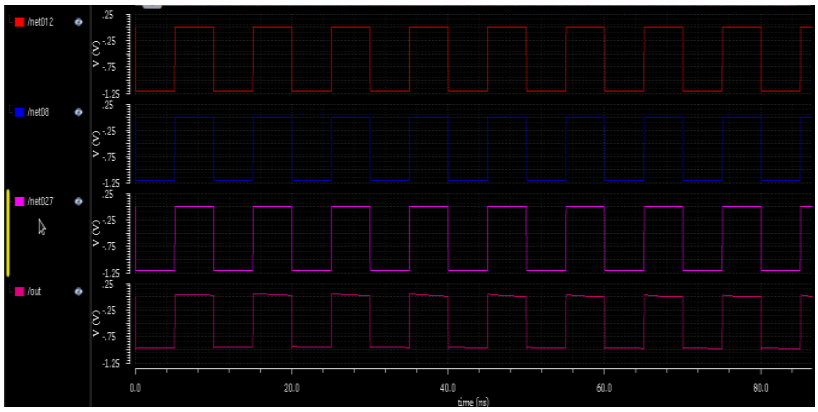

Figure 8: Simulated waveform for Logic 1 condition for 13 T SRAM cell.

As for the comparison purpose the MOS technology used is about 60 nm and the FinFET lower technology node is used in 22 nm done in Cadence Virtuoso .

Table 1

Delay Computations

Number of Transistors	CMOS(60nm)	FinFET(22 nm)
6T	1.41 W	0.98 W
13T	1.53 W	1.18 W

The delay computations of CMOS (60nm) and FinFET (22nm) are displayed in the table above . The 6T based SRAM bit-cell gives a delay of CMOS is 1.41 W whereas the delay of FINFET is 0.98 W and also by comparing the two for 13T SRAM bit-cell , it is observed that the delay of CMOS is 1.53 W and the delay of FINFET is 1.18 W .This shows how much the FinFET lower technology node is advantageous over the regular CMOS technology. Control over low leakage current with gate all around outsmarts the normal planar MOSFET . The MugFET[6] or the Multigate Field Effect Transistors is one step over the normal CMOS counterparts in many respects which is shown by mathematical calculations as well as by simulated outputs.

3. Conclusion

The circuit proposed of 13T SRAM outclasses its 6T counterpart in terms of speed and power consumption. The addition of FinFET adds more advantages as it reduces the leakage as well as proper scalability increases. This SRAM outsmarts the DRAM in many aspects . The Cadence Virtuoso is used for the design purpose. Here, in the proposed work , there is a reduction in the power and delay as the novel circuit uses FINFET and it gets one step ahead of CMOS. The 13T SRAM is much more resistant to soft errors[7] and also an ultra low power device to be used for future space related studies and applications .

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