Design and comparative analysis of a partially adiabatic and a CMOS based ALU

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Abstract

Low power VLSI design is one of the most important areas of modern digital logic design system. Designing low power systems is challenging as lowering the power dissipation can inadvertently change other parameters in the system. Conventional CMOS based systems worked well with technology sizes of a few micrometers upto a few 100 nanometers. However, as Moore's Law advanced it became difficult to design low-power systems using CMOS based design. Adiabatic logic provides an excellent alternative to traditional CMOS based design techniques, especially at lower sub-100nm technology. In this paper two arithmetic and logical units are designed using conventional CMOS technique and positive feedback adiabatic logic technique and compared primarily in terms of their dynamic power dissipation.

Keywords

ALU, CMOS, Partially Adiabatic Logic, PFAL.

1. Introduction

Low power design in VLSI is one of the primary areas in modern chip fabrication. During the process of low power design, it is essential to ensure that changes in other performance parameters do not lead to performance deterioration of the system. Some of the primary performance constraints in designing VLSI systems are power, area and speed. All these parameters are interdependent on each other. Designing systems which dissipate less power is essential to ensure system efficiency.

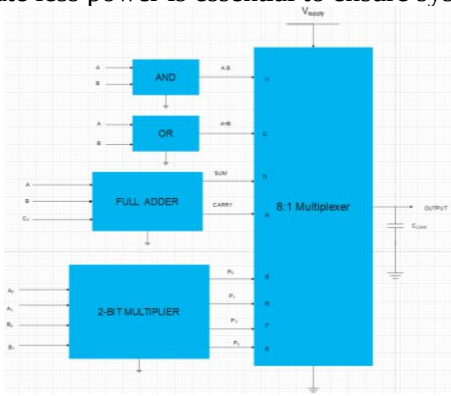

Figure.1: ALU block diagram

In this paper, an Arithmetic and Logical Unit (ALU) is designed and analyzed. Adiabatic logic is a special low-power design method which typically leads to a better performance in terms of power dissipation as compared to traditional CMOS logic. A low-power design technique called Positive-Feedback Adiabatic Logic (PFAL) is used to design the ALU and all its lower

International Conference on Emerging Technologies: AI, IoT, and CPS for Science & Technology Applications, September 06–07, 2021, NITTTR Chandigarh, India
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hierarchical components. In this paper the PFAL design is compared with the traditional CMOS based design technique primarily in terms of dynamic power dissipation. A hierarchical design method is employed to design the ALU. An 8:1 multiplexer was employed to select the desired function. Two logical functions (AND, OR) and two arithmetic functions (A Full adder and 2-bit multiplier) were designed for the ALU.

All the combinational circuit elements were designed by using MOSFETs. The block diagram of the ALU is shown in Figure 1. The entire design of the ALU is made in a hierarchical structure with Gate level systems used to design combinational blocks for the ALU.

These combinational blocks are then combined to form the complete ALU structure shown in figure 1. For the entire design of the two ALU's standard 45nm technology files were used developed by PTM and ARM [1].

2. Power Dissipation

Power dissipation in VLSI circuits can be majorly classified into two main categories: Dynamic and static power dissipation. Static power dissipation occurs when the device is turned off. The primary source of static power dissipation are the leakage currents in the transistors. Usually, static power dissipation is negligible in most CMOS systems and can be neglected. Static component of power dissipation becomes significant when dealing with technology levels reaching sub 25nm (eg. 22nm, 14nm).[6] In this paper 45nm technology levels are used throughout wherein the primary source of power dissipation is still dynamic power dissipation.

2.1.Dynamic Power Dissipation

Dynamic power dissipation occurs mainly during output switching. When the output of a digital circuit switches states the output load capacitance either charges or discharges. It is during this charging and discharging operation that most of the dynamic power is dissipated in the circuit. The dynamic power dissipation due to charging and discharging of the load capacitance can be determined by finding the product of the current through the load capacitance, I_{load} and the voltage level. Average power dissipation is computed by integrating the product in equation (1) over a time period 'T', in order to normalize and better compare the power loss between the different components throughout this paper.

$$\text{P.D.}_{\text{average}} = \frac{1}{T}\int_0^T V(t) * I(t)dt \quad (1)$$

The energy consumed in traditional CMOS logic systems can be evaluated by considering the total energy dissipated when the output switches from high to low or vice-versa. It can be evaluated as follows in Eq. (2). The amount of energy that is supplied by the power supply when the output of the system switches from low to high (0→1) is given in equation 2.

$$E_{0\rightarrow 1} = C_L {V_{DD}}^2 \quad (2)$$

Only half of this energy is available at the load of the system. The other half of the energy is dissipated by the circuit itself during the switching operation as dynamic power dissipation described earlier. As a result, the energy dissipated by the systems is given by:

$$E_{diss} = \frac{C_L {V_{DD}}^2}{2} \quad (3)$$

This is the lower limit of the energy dissipation due to output switching. In order to minimize the amount of dynamic power dissipation due to switching operation we can opt for either reducing the output load (C_L) or scaling down the supply voltage V_{DD}. It leads to a limit on the amount of load that can be driven by the system or its components. It also limits the use of higher supply voltages depending upon the tolerance of power dissipation of the system.

The following section illustrates the design of CMOS based ALU and the dynamic power dissipation of the various components involved in the design. The variation of the power dissipation

with the load is also computed.

3. CMOS based Arithmetic and Logical Unit

This section explores the design and dynamic power dissipation calculations of the various components of the CMOS based ALU. The basic structure of the ALU is the same as in figure 1. It was designed using the typical CMOS based design technique which uses the PMOS in the pull- up network and NMOS in the pull-down network [4][10]. All the components of the ALU were separately designed and analyzed and in order to select the desired input we use an 8:1 multiplexer. The components of the ALU used are: AND gate, OR gate, Full Adder (Sum and Carry) and a 2- bit multiplier. The variation of the power dissipation with the load is given in tables 1,2,3 for the various components of the CMOS based ALU.

A 2-bit multiplier is used to multiply two 2-bit binary numbers. The basic multiplication method of 2-bit multipliers is the same as the usual decimal multiplication methods. This is indicated below for two 2-bit numbers A_1A_0 and B_1B_0. After simplification the output of the multiplier in terms of the input bits is given in equation 4.

$$P_0 = A_0\, B_0 \tag{4a}$$

$$P_1 = A_0\, B_1 \oplus A_1B_0 \tag{4b}$$

$$P_2 = A_1\, \bar{A}_0 B_1 + A_1 B_1\, \bar{B}_0 \tag{4c}$$

$$P_3 = A_1\ A_0\ B_1\ B_0 \tag{4d}$$

inally, in order to select a single output at a time for the ALU an 8:1 multiplexer was employed. The mux was used to select the desired output in accordance with the applied select line signal. The power dissipation variation with the load is given in table 1.

3.1. CMOS based ALU design:

After designing all the individual components for the ALU, they were combined as shown in Fig. 1 to assemble the final structure. All the individual components were made into black boxes using SPICE and analysed as the complete ALU. The final SPICE simulation of the output waveforms and the power dissipation variation of the output stage is shown here. The inputs of the multiplexer are the outputs of the different combinational blocks designed in the preceding sections.

Table 1

Power dissipation in output of CMOS based ALU

Load capacitance(nF)	Power Dissipation(nW)
0.1	0.78315
0.2	1.887
1	5.95
2	1.8331
3	2.377
5	2.7671
10	4.7629
15	11.059
20	8.5202
50	25.359

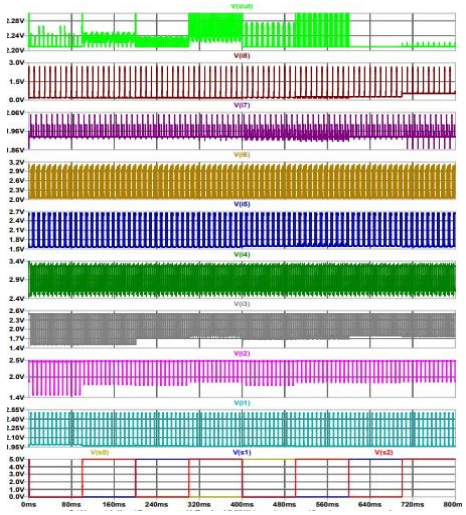

Figure 2: Output waveform of CMOS based ALU

4. Adiabatic Digital Logic

Adiabatic logic is a digital logic design technique primarily used to synthesize low-power systems. They need both the actual and complementary inputs and provide both the true and complementary outputs. Adiabatic logic design is a type of reversible logic design as the output voltages are reused to conserve power.[14] One of the major differences between CMOS and adiabatic systems is the use of the pulsed power supply in adiabatic systems [7]. The operation of all adiabatic systems can be described through the operation of the pulsed power supply designed in the next section.

In the charging phase of the pulsed power supply, the load capacitor is charged to a required level. During the hold phase, the inputs can switch and the corresponding outputs are available at the load. During the discharge phase, the energy is recovered by the system and is supplied back to the power supply to minimize power dissipation. This is one of the primary reasons why adiabatic systems consume much lesser energy in comparison to CMOS systems.

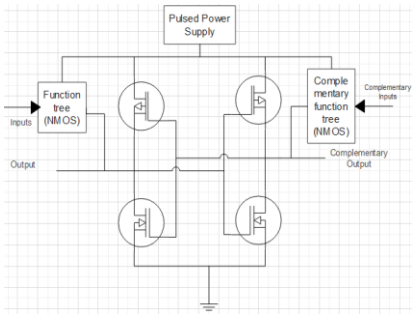

Figure.3: General PFAL structure

Partially adiabatic systems are also widely used in applications where area is a constraint. Partially adiabatic systems use a lot fewer transistors in comparison to fully adiabatic systems, while still providing most of their functionalities including lower power dissipation. The design of the ALU in the following sections uses positive feedback adiabatic logic (PFAL) which is one of the most widely used Partially Adiabatic design method. The general structure of the PFAL design methodology is shown in figure 3[3]. One of the most important aspect of adiabatic logic systems is the design of the pulsed power supply. The following section deals with the design of the pulsed power supply to be used in the adiabatic design of the ALU.

4.1.Design of Pulsed Power Supply for Adiabatic Digital Logic

The pulsed power supply is effectively a pulse or clock signal. One of the primaryreasons that adiabatic systems exhibit low power dissipation is the use of the pulsed power supply. The pulsed power supply design has major direct implications on the final power dissipation of the adiabatic circuit. In adiabatic systems it is essential to ensure that the pulsed power supply itself does not consume a large amount of power as it would make the entire design redundant.

In most of the existing pulsed power supply designs a synchronous or asynchronous oscillator system are used. A few of those designs are described here [3][15]. In this paper instead of using the already existing pulsed power supply designs in literature, some modified designs have been considered. Two of those designs are described in the following sections.

4.1.1. LC oscillator based pulsed power supply.

A modified Colpitts Oscillator was used as the pulsed power supply for the adiabatic system. The design is shown in figure 4.

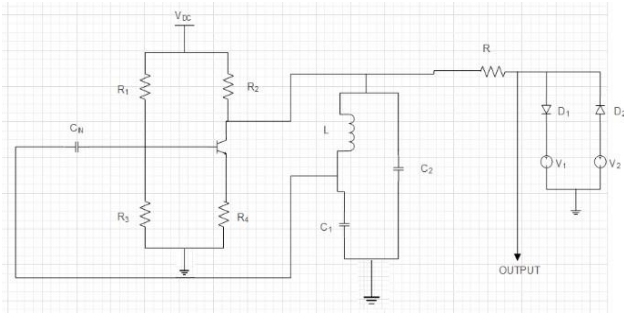

Figure 4: LC oscillator based pulsed power

This design used an amplifier stage followed by an LC oscillator stage and finally a clipping circuit. The first stage is used to provide the gain or amplification using a voltage-divider bias using BJT. The next stage is the LC oscillator stage which determines the frequency of the pulsed power supply. The output of this stage is sinusoidal [5].

However, as we require a pulse waveform for the adiabatic system, a clipping stage is added with 2 diodes and 2 voltages to control the amplitude as required. In order to modify the amplitude of the signal the clipper voltage levels (V_1 and V_2) need to be adjusted.

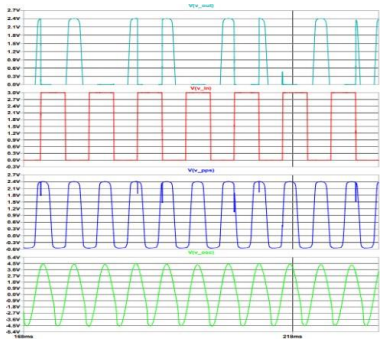

Figure 5: Output waveform of inverter using LC oscillator based Pulsed power supply

The amplitude decides the final level of the supply voltage to be used for the adiabatic system. This design worked well with simple PFAL circuits. This design was used for a PFAL inverter the

output waveform of which is shown in figure 5.

There were a few drawbacks observed for this design. Despite a relatively stable output pulsed waveform initially, this pulsed power supply proved to be difficult to operate for more complex systems which was majorly due to the difficulty in controlling the frequency and amplitude of the pulsed signal. The frequency of the waveform depends upon the LC branch of the power supply given by the following expression [16]:

$$f_0 = \frac{1}{2\pi\sqrt{L\frac{C_1C_2}{C_1+C_2}}} \tag{5}$$

In order to modify the frequency of the pulse we need to replace the existing components or design them in a way such that they can be adaptive. Also, it is important to ensure that the variations in the pulsed power supply do not interfere with the output waveform. This can be ensured through a more stable pulsed output and adjusting it in a way that the charging or discharging cycle of the power supply do not coincide with the switching outputs. As the design is highly dependent upon the oscillator and clipping mechanism used, this makes the design rigid and proved to be difficult to operate for more complex ALU components. The lack of portability of this design would not be suitable for more complex adiabatic systems where the frequency and amplitude of the pulsed power supply is extremely essential.

4.1.2.Current-source and capacitor-based PPS

In order to overcome the drawbacks of the oscillator based pulsed power supply design, a second different design was then used to design the pulsed power supply. This design used a piecewise linear current source which would charge a suitable capacitor. The output voltage of the capacitor would be used as the pulsed power supply. A diode was also added to protect the power supply from reverse voltages from the circuit. The basic structure of the supply is shown in figure 6. In order to shape the supply in the form of a pulse, as required by adiabatic systems, the current source needs to be selected in such a manner that it charges the capacitor and the capacitor in turn provides an output voltage which is in the form of a pulse signal. This pulsed waveform is finally used for the adiabatic logic components.

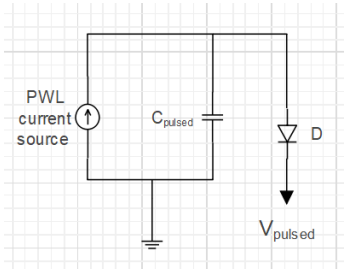

Figure 6: PWL current source-based PPS

A current source of the form shown in figure 7(a) is used to form the pulsed source. Three cases are possible as the waveform may be divided into 3 main components i.e. when a positive constant current is applied, when the direction of the current is reversed and when the current is turned off. Here $V(t_0)$ is the initial voltage of the capacitor assumed to be zero in this case. The voltage across the capacitor is given by the following expression which is linear.

$$V_c(t) = \frac{I}{C}t \tag{6}$$

Similarly, for case (2) we get the voltage across the capacitor as:

$$V_c(t) = -\frac{I}{C}t \tag{7}$$

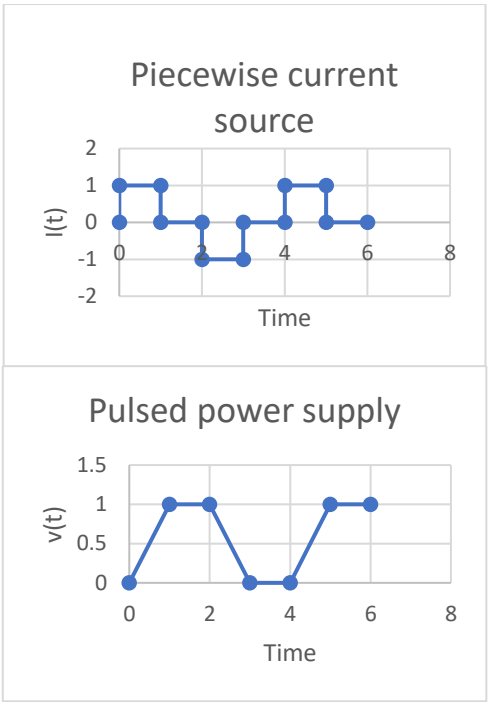

Figure 7: Pulsed power supply generated through a PWL current source.

Which is linear with a negative slope. In case (3) when the current source is switched off the capacitor is charged to a certain voltage and would ideally remain at that voltage until the next discharge cycle or if it encounters lossy circuit element. The corresponding voltage waveform which appears across the capacitor is as given in figure 7(b). This capacitor-based power supply helped to overcome the lack of flexibility in controlling the amplitude and frequency of the pulse encountered in the oscillating power supply in section 4.1.1. Another advantage of this type of power supply was the simplicity in design, as it needed very minimal components. For the rest of this paper this supply is used for the various adiabatic circuit components.

4.2.Minimizing power dissipation in adiabatic circuits

For the entire ALU design including all its components the power supply designed in the previous section is used. However, in order to ensure the power dissipation of the partially adiabatic design is lesser than the traditional CMOS based design there are certain parametric constraints which need to be considered.

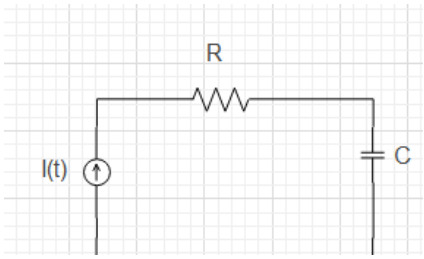

Figure 8: Adiabatic charging of a capacitor

To reduce the power dissipation in adiabatic circuits we use a special type of charging method called adiabatic charging. The simplified model of this charging method can be described using a capacitor

charging through a current source I(t) as shown in figure 8.[8]
The voltage across the capacitor is:

$$V_c(t) = \frac{1}{C} I(t)t \quad (8)$$

The energy dissipated by the resistor in time 'T' is given by:

$$E_{diss} = \frac{RC}{T}(C(V_C(T)^2) \quad (9)$$

From equation 3 we saw that the lower limit of power dissipation in conventional CMOS circuits was found to be $E_{diss} = \frac{C_L V_{DD}^2}{2}$.
So, if we compare equation 9 with equation 3 it can be concluded that in order to minimize the power dissipation in adiabatic systems, compared to conventional CMOS systems, we need to satisfy the following inequality:

$$T > 2RC \quad (10)$$

When this inequality is satisfied the energy dissipated in adiabatic circuits can be reduced below the lower limit of conventional CMOS circuits. Here, T is the time taken to charge up the capacitor C using the pulsed power supply which was designed in the previous section. Therefore, to minimize the power dissipation we need to ensure the time taken to charge up the capacitor is at least larger than 2RC. This time is depicted in figure 7. The load used in the design is in the order of a few nanometers and the typical values of MOSFET on-resistances is in the order of a few ohms [9][11-12]. As the transient charging time of the capacitor is kept at a few milliseconds this ensures that the expression given in (12) is satisfied.

4.3. Adiabatic logic based ALU

Similar to the CMOS based ALU designed in section 3, a PFAL based ALU was designed which comprised of the same components as the CMOS design. As described in the previous section, there are limitations on the pulsed power supply voltage which can be used depending upon the value of internal resistances and the load capacitance. The following are the SPICE simulations of the components of the PFAL based ALU and the average dynamic power dissipated. All the implementations use the current source-capacitor based Pulsed Power Supply which was designed in section 4.1.2. The tables below summarises the power dissipations of these components.

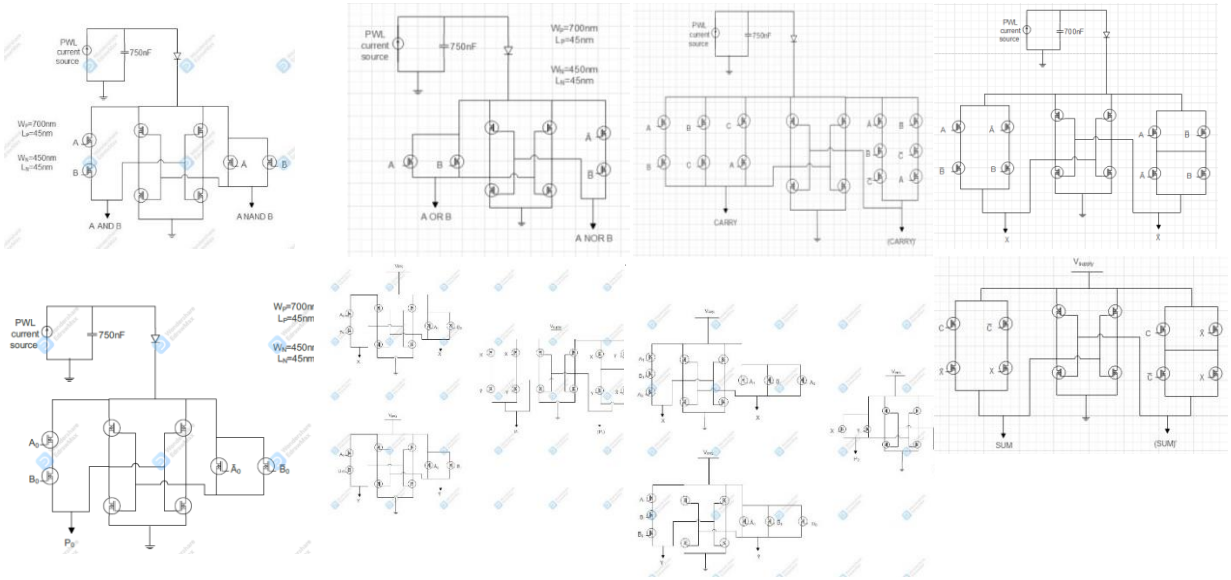

Figure 9: SPICE simulation of the ALU components used in the PFAL design methodology: AND gate, OR gate, Sum and Carry blocks of the full adder and the 4 input blocks of the 2-bit multiplier.

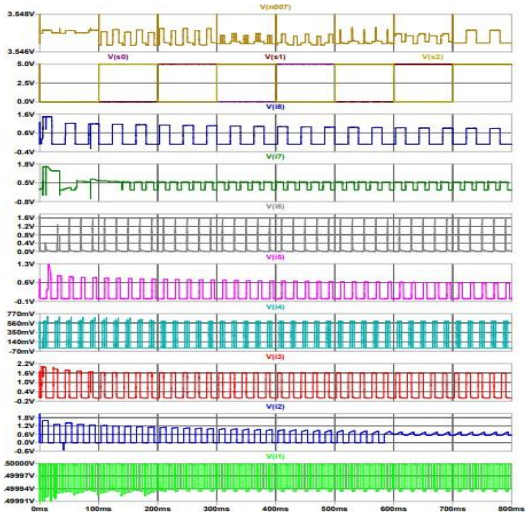

Figure 10: Output waveform of PFAL based ALU

Finally, to select the output, an 8:1 mux was designed. The SPICE schematic of the output waveforms is shown in figure 10 and the corresponding power dissipation variation is shown in table 2. All the combinational blocks designed in the previous sections were combined to form the PFAL based ALU which followed the same basic design structure as shown in Fig.1. The output waveform of the ALU is shown in figure 12 and the corresponding power dissipation of the output stage variation is shown in table 8.

Table 2:

Power dissipation of the output stage of PFAL based ALU.

Load capacitance(nF)	Power Dissipation(nW)
0.1	0.036522
0.2	0.041377
1	0.13306
2	0.022205
3	0.11942
5	0.08129
10	0.20715
15	0.18535
20	0.48261
50	0.59726

5. Results

The following diagram illustrates the difference in power dissipation with the load between the two logic styles when operated at similar supply voltages for the two ALU design methodologies. There is a strong dependance of the amount of dynamic power dissipated on the load used for the circuit. This can be clearly seen in the graph in Figure 11.

It can be seen that the PFAL based components have a significantly lower dynamic power dissipation as compared to their CMOS counterparts. The use of the capacitor and current source based pulsed power supply along with the PFAL design structure were the primary reasons for the reduced dynamic power dissipation in the PFAL based system. As PFAL is a reversible design methodology, it is excellent for low-power applications.

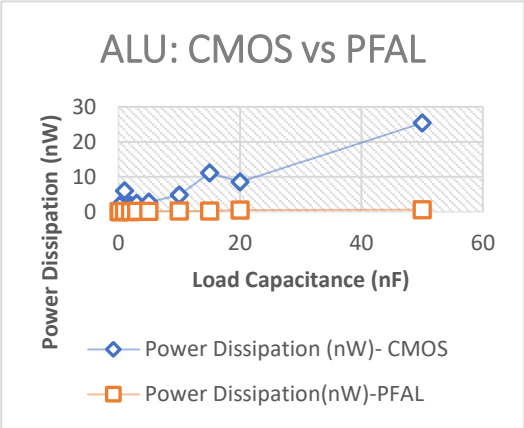

Figure 11: Variation of dynamic power dissipation in the two design styles for the ALU when the load is changed.

In this paper a partially adiabatic design and conventional CMOS based design techniques were compared through a number of combinational circuits. The combinational circuits were in turn used to design an Arithmetic and Logical Unit.

The overall power dissipation in adiabatic system was found to be much lower as compared to conventional CMOS based systems as indicated in the diagrams above. In order to achieve lower power dissipation in adiabatic systems the design of pulsed power supply is essential. In this paper a current source and capacitor based pulsed power supply was designed which can be used in place of the more often used LC oscillator-based power supplies. Whenever there are constraints in terms of power dissipation, partially adiabatic systems should be preferred as they provide much lesser power dissipation without increasing the chip area by a large factor.

6. References

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