Impact of Fin Aspect ratio (T_k/L_g) on FinFET Characteristics using Compound gate Dielectrics

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Abstract

In FinFET devices, the high-k gate dielectric materials have been considered as alternative to SiO_2 for reducing leakage current, diminishing short channel effects and improvingthe effective carrier mobility. In this work, various compound gate dielectric materials have been integrated with 14nm Silicon on insulator FinFET devices. The performance of these structures have been analysed in the term of fin aspect ratio (gate dielectric thickness to gate length). The impact of this ratio on electrical performance parameters of FinFETs at ultra-low power has been deliberated. It has been inspected that the fin aspect ratio for lanthanum doped zirconium oxide has significantly dwindled, SS by 22%, DIBL by 85% , raised I_{ON}/I_{OFF}ratio in order of 10^9 andenhanced $g_m$by 1.15 times as contrast to conventional FinFET.

Keywords

FinFET, Transconductance, Subthreshold Swing, Leakage current, Dielectric permittivity.

1. Introduction

Nowadays, several miniature devices have been devised to meet the need of industry oriented applications such as higher speed transistors with low power consumption. It was inspected that FinFET device shows noticeable reduction in short channels, utilized less power and improves switching activity compared to other devices [1-3]. In transistor manufacturing processes, the several semiconductor industries such as Intel, IBM, Samsung, and TSMC has started using high-k gate oxide and metallic gate materials for scaled devices. According to ITRS reports, the scaling of gate dielectric material, SiO_2 (k=3.9) below 2nm has resulted in high leakage current due to generation of direct tunneling gate off-current [4-6]. Therefore, for prevention of this negative effect in sub-22nm technology, various novel materials such as Al_2O_3 (k=9), ZrO_2 and HfO_2 (k=25), Ta_2O_5 (22) and CeO_2 (23-26) have been widely used in microelectronic devices. The important properties of these insulating materials involve high energy band gap,chemically compatible with Silicon and high crystallization temperatures. The energy band-gap of few materials such as SiO_2 (9eV), Al_2O_3 (6eV), HfO_2 (6eV), La_2O_3 (5.18eV) and ZrO_2 (5.8eV) have been lying in the range of 4-12eV [7-13]. The good electrical characteristics using $La_2Hf_2O_7$ (LHO) high-k dielectric in place of SiO_2 has been proved as prominent candidate. Excellent transistors with enhanced performance based on Hafnium based gate dielectrics as the insulation layers

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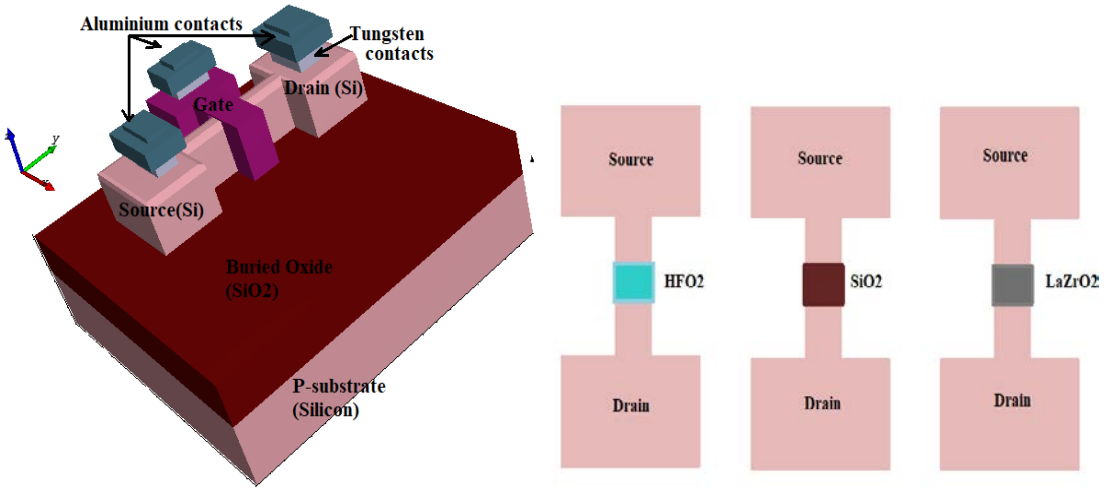
have been achieved [14-16].For future scaled devices, a gate dielectric material with$LaZrO_2$(k= 40) is preferred for below 22nm node FinFET [17-19]. In this work, the different composite high-k gate dielectric materials have been used for designing the 14nm SOI FinFETs. Theelectrical performance of these devices has been analyzed in the term of fin aspect ratiofor 1.1 and 1.6nm gate oxide thickness.
This paper is framed as follows: Section 2 explains the description of design of device and simulation framework; Section 3 discusses the device characteristics for digital parameters; last section describes the conclusion of work.

2. Device Structures and Methodology

The three dimensional structures of n-channel FinFETs (NFinFET) for different high-k materials are shown in Figure 1. Table 1 illustrates the NFinFET design parameters [20]. Device simulation is performed with Cogenda Technology Computer Aided Design (TCAD) physical simulator at 300K. The gate dielectric permittivities vary from 3.9 to 40 [21, 22] and the gate work-functions for all devices are kept at 4.6eV [23]. The potency of the simulator is examined by matching results of simulated work with published experimental data. It has been observed that our results are in good agreement with Andrade et al. [24] as shown in Figure 2. Therefore, it shows that the models and parameters used in this paper are valid. The devices have been designed with Drift diffusion model (DDM), Kane's Model, Lucent Mobility Model and SRH Model[25]. Figure 3 describes the NFinFET transfer characteristics for L_g=14nm, k= 3.9 to40, V_g=0 to 0.75V and V_d=0.75V.



(a) SOI NFinFET (b) Devices with different high-k materials

Figure 1: Structure of SOI NFinFET for different high-k materials

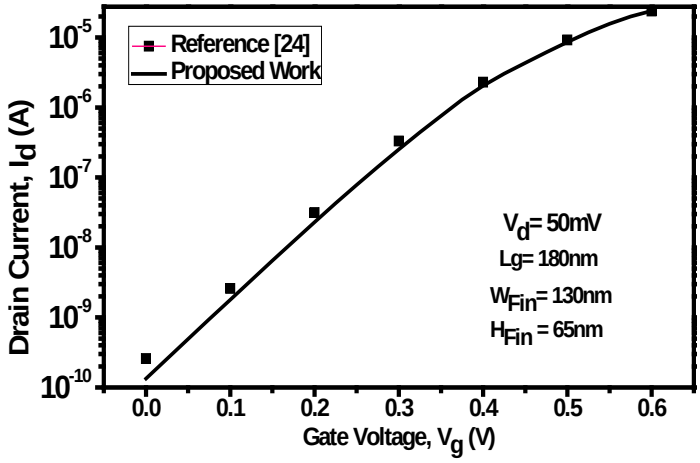


Figure 2: Transfer characteristics of proposed FINFET and reference FinFET [24]

Table 1:NFinFET design parameters

Device's Performance Parameters	Proposed device(NFinFET)
Length gate terminal, L_g(nm)	14
Fin Pitch of transistor (nm)	42
Fin Width of transistor (nm)	8
Fin Height of transistor (nm)	24
Work function of gate terminal (eV)	4.6
Gate dielectric permittivity , k	3.9 - 40
Physical Oxide Thickness(nm)	1.1,1.6
Supply Voltage (Volts)	0.75

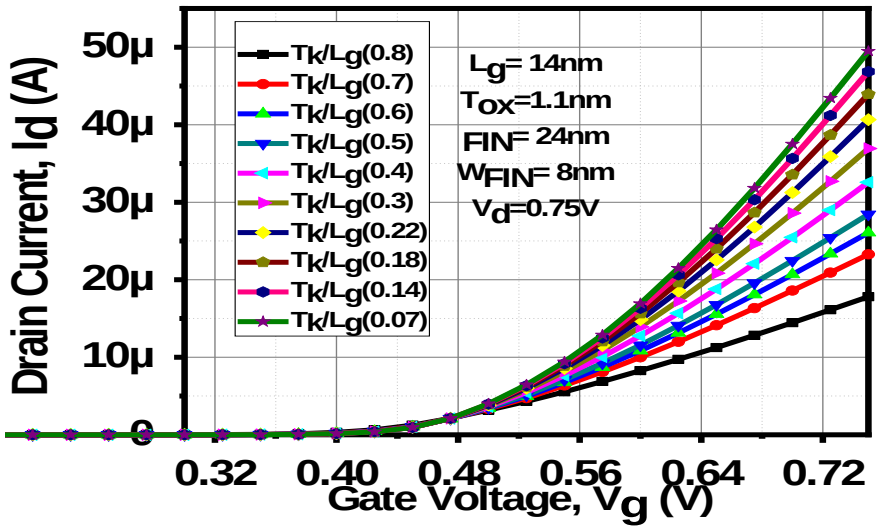


Figure 3: NFinFET Transfer characteristics for L_g=14nm, k =3.9 to 40, V_g= 0 to 0.75V and V_d=0.75V.

3. Result and Discussions

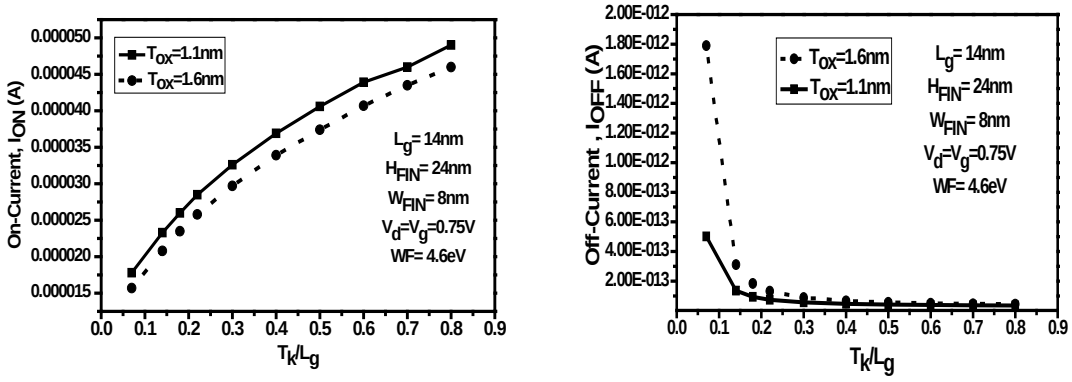
The defined range of novel gate oxide materials viz. Silicon nitride (Si_3N_4, k=7), Aluminium oxide (Al_2O_3, k=9), Hafnium silicate ($HfSiO_4$, k=11), Yttrium oxide (Y_2O_3, k=15), Hafnium oxide (HfO_2,k=20-25), Niobium pentaoxide (Nb_2O_5, k=35), and lanthanum doped zirconium oxide ($LaZrO_2$, k=40) are integrated with FinFET device. These materials have high k values (7-40), more energy band gaps, chemically compatible with Si as compared to SiO_2. Moreover, these materials can be deposited at high temperature on a silicon active channel using ALD and CVD methods [17-19, 26].The influence of fin aspect ratio on device characteristics have been demonstrated below using these novel materials.

3.1. Impact of Fin Aspect ratio (T_k/L_g) on Device Characteristics

The impact of fin aspect ratios on FinFET's digital device performance metrics such as Off- current (I_{OFF}) ,current ratio (I_{ON}/I_{OFF}),On-current (I_{ON}), Drain-induced BarrierLowering(DIBL), Subthreshold swing (SS), transconductance (g_m) are discussed through TCAD simulation [12, 27-29]. The aspect ratio for a given 'k' is solved by $T_k/L_g = \{ (k/3.9) \times T_{ox} \}/L_g$, where $T_{ox}$is gate oxide thickness, T_k is gate dielectric thickness, 3.9 is SiO_2 dielectric constant and L_g is gate length. The range of k is taken from 3.9 to 40 for gate oxide thickness of 1.1nm and 1.6nm [21].

3.1.1. I_{ON} and I_{OFF} currents

Figure 4 (a-b) demonstrates that on-current (calculated at $V_g=V_d=0.75V$) enhances and off-current (determined at $V_g=0$, $V_d=0.75V$) reduces with the increase in aspect ratio. Furthermore, on-current and off-current improvement is more for T_{ox} =1.1nm as compared to T_{ox} =1.6nm. This is convenient to understand, as the narrow gate oxide has greater command over the channel region and thereby superior performance at short channel [18, 30]. The maximum on-current and minimum off-current is obtained for highest T_k/L_g ratio (k=40, $LaZrO_2$).



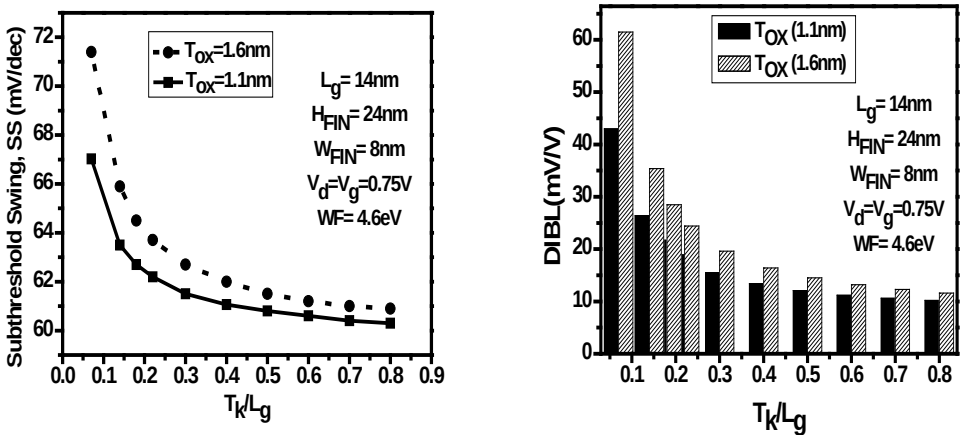
(a) (b)

Figure 4. The influence of compound gate dielectric on (a) I_{ON} and (b) I_{OFF} for oxide thickness of 1.1nm and 1.6nm. (Fin aspect ratio is calculated as T_k/L_g= (k/3.9)*(1.1 or 1.6)*(1/14).

3.1.2. DIBL and SS

DIBL signifies the decrease of the cut-in voltage of device at higher drain voltages [12]. SS shows fluctuations in drain current corresponding to gate voltage. The theoretical value of SS is 60mV/dec at 300K. As the gate dielectric permittivity increases, the gate capacitance rises which results in reduced SS and DIBL as shown in Figure 5 [12, 30, 31].The SS and DIBL for FinFET with

$LaZrO_2$ as gate dielectric oxide obtains 10% and 76% reduction for T_{ox} =1.1nm as compared to SiO_2 gate oxide material and for T_{ox} =1.6nm the same metrics are declined by 14% and 70% respectively.Lesser DIBL and reduced SS results in low leakage current and better on/off switching performance, respectively [31].

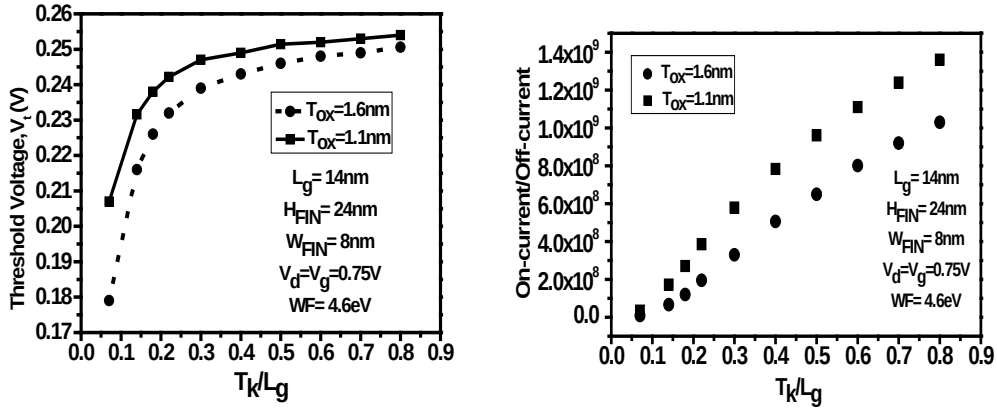


(a) (b)

Figure 5. Influence of aspect ratio (T_k/L_g) of given k dielectric permittivity on (a) SS and (b) DIBL for oxide thickness of 1.1nm and 1.6nm.

3.1.3. I_{ON}/I_{OFF} and Threshold Voltage (V_t)

The V_t is one of the important parameters characterizing the behavior of metal-insulator-semiconductor interfaces in FinFET structures. To extract the value of V_t, the constant current method is used [32]. The influence of compound gate dielectric permittivity on threshold voltage and the current ratio I_{ON}/I_{OFF} as shown in Figure 6 implies that thinner gate oxide (T_{ox}=1.1nm) has higher current ratio and larger V_t as compared to thicker gate oxide (T_{ox}=1.6nm). It is also interesting to note that I_{ON}/I_{OFF} is increasing with increasing V_t for both gate oxide thicknesses. An I_{ON}/I_{OFF} of order of 10^9 for higher dielectric gate oxide materials indicates that V_g has greater control over the operation of MOSFET as compared to V_d. Therefore, it is recognized that device with thin gate oxide thickness and high-k gate dielectric permittivity is suitable for the implementation of VLSI circuits [33-35].



(a) (b)

Figure 6. Dependence of (a) V_t and (b) I_{ON}/I_{OFF} on the aspect ratio (T_k/L_g) for varied k of 1.1nm and 1.6nm gate oxide thickness.

3.1.4. Gate Transconductance

The gate transconductance, g_m is defined as ratio of drain current variation and gate voltages variation at a constant drain voltage ($g_m=\partial I_d / \partial V_g$). It is expressed in the Siemens unit (S). It is observed that thicker gate oxide has lesser g_m as outlined in Figure 7. The highest magnitude of g_m decides the gain and operating speed of a transistor [33-35].

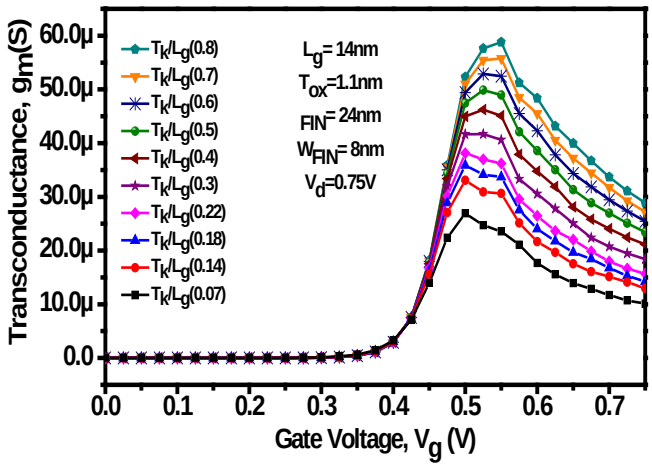


Figure 7: Transconductance trend for variable dielectric permittivity (k) of T_{ox}=1.1nm.

4. Conclusion

The impact of fin aspect ratio on the electrical performance of compound gate dielectric based FinFET devices have been analyzed in Cogenda TCAD environment with drift-diffusion transport framework. It is found that the device proposed with higher fin aspect ratio demonstrates superior SCEs immunity. The SS and DIBL for FinFET with lanthanum doped zirconiumas gate dielectric oxide obtains 10% and 76% reduction for T_{ox} =1.1nm as compared to SiO_2 gate oxide material and for T_{ox} =1.6nm the same metrics are declined by 14% and 70% respectively. It has been inspected that the fin aspect ratio of $LaZrO_2$ for T_{ox} =1.1nm has significantly dwindled SS by 22% , DIBL by 85%and I_{ON}/I_{OFF} is increased in order of 10^9 over 10^7 as compared to work done in previous literature [36]. The notable enhancement for g_m showsits suitability in VLSI applications as an inverter circuit

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