Design of Ternary Decoder

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Abstract

The analysis of advantages of ternary logic on an example of construction of ternary RS-trigger is considered. Based on the multi-threshold element of multi-valued logic (MTEML), the structures of the different variants of single-input decoders with the different active levels are proposed. The structures of the obtained elements and their schemes for the selection of the simplest variants are analyzed.

The future directions of work and expediency of development of subjects of construction of ternary elements and systems on their basis are outlined.

Keywords

Ternary logic, multi-threshold element of multi-valued logic, methods of constructing ternary elements, decoder

1. Introduction

The relevance of the topic is due to the fact that modern computer technology needs new ways to increase computing power and speed. Binary logic is now the most common, but it has a number of disadvantages that can be eliminated through the use of ternary logic, including increasing the range of numbers, speeding up operations, reducing the amount of equipment.

The purpose of the work is the design and synthesis of logical elements for ternary computer systems.

Three-valued logic is more convenient and familiar to people than two-valued logic [1]. Consider some examples that prove this.

The first example is the weight of the levers (Fig. 1). They are a characteristic ternary device, the three states of which correspond to three possible relations: A> B, A = B, A <B. For comparison, consider also the executive scales, which can take only two states, corresponding, for example, the ratio A> B, A≤B (Fig. 2). It is clear that binary scales are less convenient than ternary. Only in the case of A> B the result of weighing on them is determined immediately, and in the other two cases it is necessary to re-weigh by swapping A and B [2].

Figure 1: Ternary scales

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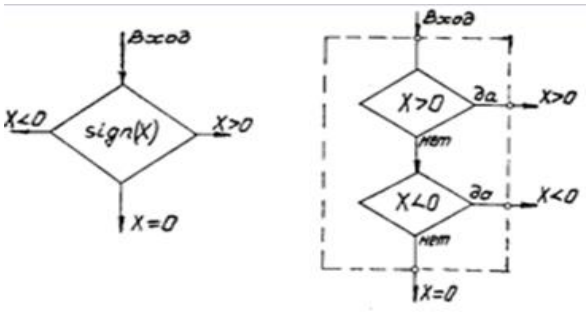
Figure 2: Binary scales

The next example is branching by the sign of the variable x (Fig. 3). This example demonstrates the fundamental difference between three-digit logic and two-digit logic. It is that one and the same can be represented in a more compact form in ternary logic than in binary. In this example, the ternary branching by the sign x is described by specifying a single three-digit operation sign (x) and is performed in one step, while the same branching, which is carried out by means of two-digit logic, associated with the need for two operations and is performed by two steps. Such branching algorithms are often used in decision-making systems, in "Smart Homes" to process signals from sensors and the corresponding response to them. Ternary logic in this case will significantly accelerate this reaction [3].



a) b)

Figure 3: Branch operation by sign: a) ternary scheme; b) binary scheme

These examples show that ternary logic allows you to reason more simply and more quickly than reasoning in terms of ambiguous logic [4]. In practice, people probably use mostly ternary logic [5,6].

Some properties of ternary logic determine its effectiveness and practical value:

- the branching command by sign takes twice less time than in binary;
- the ternary adder subtracts when inverting one of the terms, from which it follows that the ternary counter is automatically reversible;
- in the three-input ternary adder the transfer to the next category occurs in 8 situations out of 27, and in the binary adder - in 4 out of 8;
- the three-level signal is more resistant to interference in transmission lines. This means that special methods of redundant coding of ternary information are simpler than binary [7].

2. Ternary RS-trigger

In addition to combinational circuits, the output state of which at each time depends on the set of input signals, in computer systems are widely used circuits and nodes in which the output state depends not only on the input signals but also on their previous state, ie digital automata. As you know, the simplest device with two stable states at the output - the trigger is often used to store information.

Consider binary and ternary RS-flip-flops in comparison.

Figure 4 shows the designation of the binary RS-flip-flop.

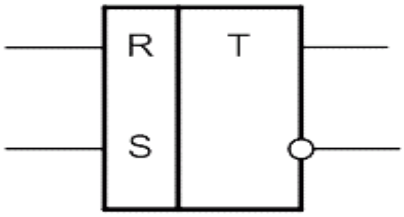


Figure 4: Designation of a binary RS-trigger

The trigger has 2 states Q = 0 and Q = 1, which are displayed on its outputs. The next state of the trigger depends on the current state and the combination of input signals at its two inputs.

It is known that it has a forbidden combination of input signals. If there are active signals S = 1, R = 1 on both inputs at the same time, this mode is considered forbidden, because the state of the trigger will not be determined.

In ternary logic, three allowed modes can be provided with only one input [8]. In this case, in addition to reducing the number of pins, such a device in principle cannot be the fourth, forbidden mode. Based on MTEML the ternary RS -trigger which scheme is shown in fig. 5.

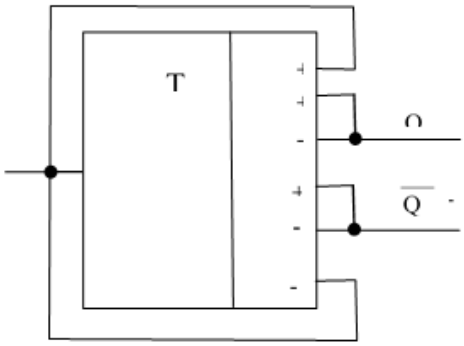


Figure 5: Scheme of ternary RS-trigger

Feedback from the + R, -R outputs provides support for the current state of the trigger in the absence or zero value of the input signal. The input signal "+" leads to the transition of the trigger to the state "+", the signal "-" to the transition to the corresponding state "-". The ternary RS-flip-flop has another state "0", but it is unstable and is possible only when the system is initially turned on (Table 1).

When applied to the input x = 0 - the trigger is in storage mode, its state does not change. When applied to the input x = - 1 (minus) the trigger goes into reset mode, ie the output will also be minus 1, when x = + 1 the trigger goes into installation mode and the output is also +1. The state of the trigger, when the signal at its output is zero, and the input is a non-zero value (either "+" or "-") is unstable, and immediately changes depending on the signal sign. Table 1 shows the previous and subsequent states of the trigger.

Table 1

Truth table of the ternary RS-trigger

№	X	-r +r	q	X; – r; +r	-R1 +R1	Q = -R1; +R1
0	–	– 0	–	- -	– 0	–
1	–	– +	0	–	– 0	–
2	–	0 +	+	0	– +	0
3	0	– 0	–	–	– 0	–
4	0	– +	0	0	– +	0
5	0	0 +	+	+	0 +	+
6	+	– 0	–	0	– +	0
7	+	– +	0	+	0 +	+
8	+	0 +	+	+ +	0 +	+
0	–	– 0	–	- -	– 0	–
1	–	– +	0	–	– 0	–

In principle, a ternary RS-flip-flop can have three different states of input and three different states of output signals, i.e. nine combinations, which are represented by terms in the table. The input signal is denoted by X, the signals of the current state and their sum - the current state are denoted by lowercase letters -r, + r, q, respectively. The signal that is directly generated at the input of the trigger is equal to the sum of these signals and is indicated in the table by column X; -r; + r, this signal determines the next combination of output signals -R, + R and the next state Q = -R; + R, which trigger will go.

3. Ternary single-input decoders

Decoders are a must-have for any computer system. They are more commonly used to identify address space and are used to select specific devices or memory cells when addressing them (setting the address on the appropriate bus).

In fact, decoders convert the input code of a given number system to unary, in which the output active signal is present only on one of the outputs, the number of which corresponds to the input combination. The maximum number of outputs for a ternary decoder is $m = 3^n$, where n is the number of inputs. Consider the construction of one- and two-input ternary decoders.

For a single-input decoder, the number of outputs is three. Depending on what value of output signals we will consider active, and what passive - there can be six different combinations and, accordingly, schemes of construction of one-bit ternary decoders. To build decoders we use MTEML. The table 2 shows the values of the outputs of the element depending on the signal at the input X.

Table 2

Values of the outputs of the MTEML

X	-L	-R	+L	+R
-	0	-	+	0
0	0	-	0	+
+	-	0	0	+

On the basis of MTEML variants of a ternary one-input decoder with various active signals which structural schemes are shown in fig. 6-11.

Consider a decoder whose active value is "-", passive value "0". The truth table for each of the three outputs is presented in the table 3.

Table 3
Decoder truth table

X	Y0	Y1	Y2
-	-	0	0
0	0	-	0
+	0	0	-

It is easy to conclude that to obtain three output signals you need to combine the following outputs of MTEML:

Y0= -R, +R, -L = -1, +R

Y1= -R, +L

Y2=-L

To simplify the implementation of the outputs -R, -L, which are equal to "-1", regardless of the input signal, replace the corresponding current source. We obtain the scheme shown in Fig. 6.

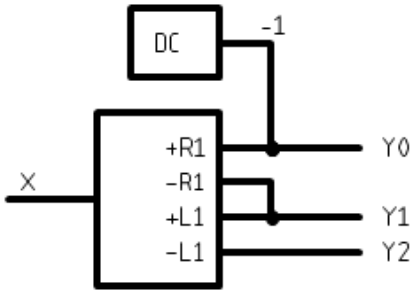


Figure 6: Block diagram of a single-input decoder with active "-"

The following truth table (Table 4) shows the case of the active signal "+", passive "0".

Table 4
Decoder truth table

X	Y0	Y1	Y2
-	+	0	0
0	0	+	0
+	0	0	+

The following are expressions for constructing outputs by combining and simplifying the corresponding signals. In fig. 7 shows a diagram that implements this.

Y0= +L

Y1= +R, -L

Y2= +R, -R, +L = +1, -R

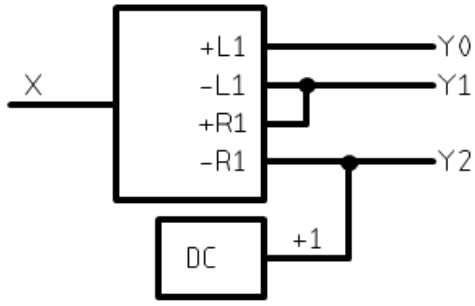


Figure 7: Block diagram of a single-input decoder with active "-"

Tables 5 - 8 show the output signals for the cases of active "0", passive "-" (Table 5), active "0", passive "+" (Table 6), active "-", passive "+" (Table 7) and active “+”, passive “-” (Table 8).

Figures 8 - 11 show the implementation schemes for all these cases.

Table 5
Decoder truth table. Active signal "0"

X	Y0	Y1	Y2
-	0	-	-
0	-	0	-
+	-	-	0

Y0= -L, -R, +L = -1, +L

Y1= -L, -R, +R, -L = -1, +R, -L

Y2= -R

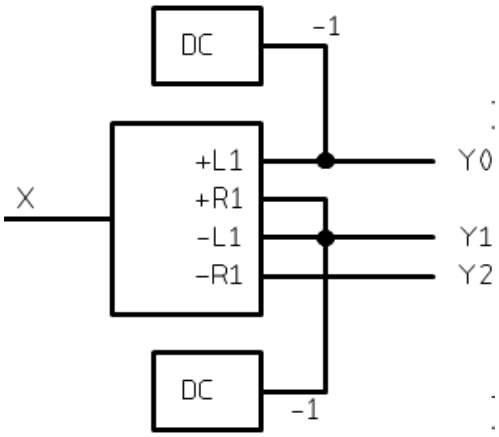


Figure 8: Block diagram of a single-input decoder with active "0", passive "-"

Table 6
Decoder truth table

X	Y0	Y1	Y2
-	0	+	+
0	+	0	+
+	+	+	0

Y0= +R
Y1= +L, +R, -R, +L = +1, -R, +L
Y2= +L, +R, -L = +1, -L

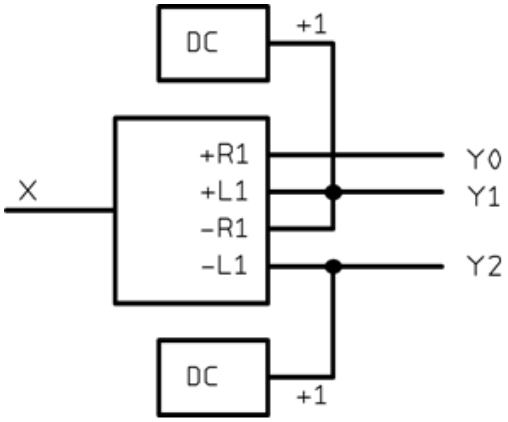


Figure 9: Block diagram of a single-input decoder with active "0", passive "+"

Table 7
Decoder truth table. Active signal "-"

X	Y0	Y1	Y2
-	-	+	+
0	+	-	+
+	+	+	-

Y0= +R, -R, +R, -L = -1, +R, +R
Y1= +R, +L, -L, -L = +1, -L, -L
Y2= +1, -R, -R, +L, +L

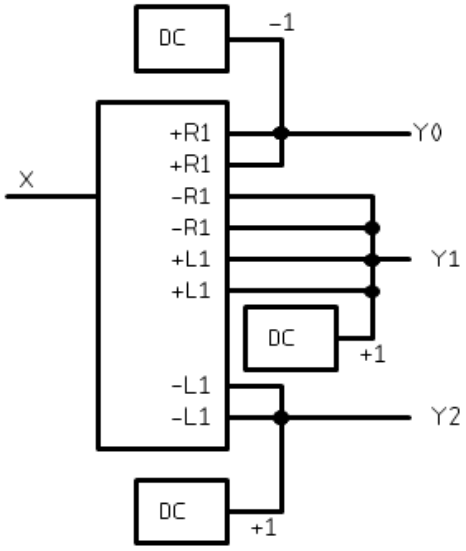


Figure 10: Block diagram of a single-input decoder with active "-"

Table 8
Decoder truth table Active signal "+"

X	Y0	Y1	Y2
-	+	-	-
0	-	+	-
+	-	-	+

Y0= -1, +L, +L
Y1= -1, +R, +R, -L, -L
Y2= +1, -R, -R

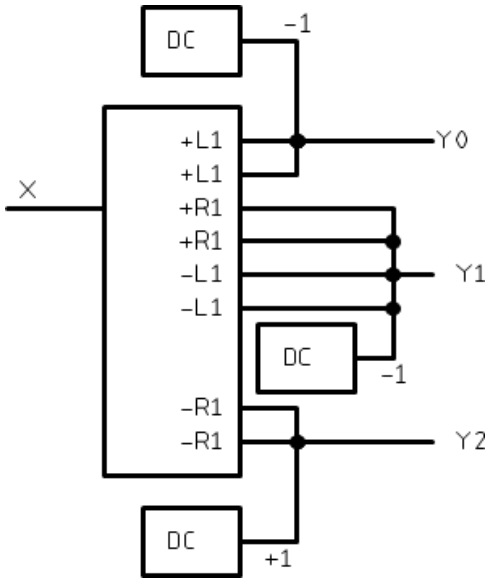


Figure 11: Block diagram of a single-input decoder with active "+"

Analysis of the obtained structures of single-input decoders showed that the simpler options are when the active signal is "-" or "+", and passive is "0".

4. Conclusions

The analysis of the construction of multivalued logic and its elemental base allowed us to draw the following conclusions.

The vast majority of the implementation of ternary elements has significant disadvantages.

These solutions either do not allow the full implementation of ternary logic, or do not have a general approach to its implementation, or complicate the implementation of ternary devices and their structure.

One of the obstacles hindering the development of ternary technology is the lack of element base and a common approach to the implementation of components and elements of non-binary computers.

The implementation of ternary devices based on threshold logic is a way to create ternary devices that can compete with binary in terms of equipment.

An urgent scientific and practical task is to create a general approach to the implementation of ternary nodes and methods of synthesis of ternary logical and arithmetic elements, as there are still no standards in the development and implementation of ternary elements and a single methodological approach.

Thus, for the first time, the structures of several variants of one-input decoder with active signals "-", "+" and "0" based on MTEML, which can be used in the construction of elements of ternary computer systems, were obtained.

The built devices have a much simpler architecture compared to their counterparts.

Analysis of the obtained structures of single-input decoders showed that the simpler options are when the active signal is "-" or "+", and passive is "0".

To build ternary computing and intelligent systems, it is necessary, first of all, to develop the principles of a systematic approach to the synthesis of ternary elements and software for their interaction with each other and with existing modern devices.

Therefore, in further research it is expedient to consider methods of construction and synthesis of nodes of ternary computer systems, their optimization, and development of principles of mathematical modeling and software of such systems and their elements.

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