Possible Ways to Improve Performance of MOSFET and Challenges

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Abstract

This paper introduced possible ways to improve the MOSFET performance from the perspective of structure and material. The two updated MOSFET models fin field-effect transistor (FinFET) and gate-all-around field-effect transistor (GAAFET) are used to derive the conclusion in this word. To improve structure-based performance, results from simulations show short channel effect and self-heating effects are to be minimized. Strain engineering is studied with material analysis. This paper concluded that performance of FET can be improved by improving the mobility of electrons or holes by changing crystal lattice structure from the perspective of strain engineering. Other than that, changing structure to minimize short channel effect, making channels more spherical shape, and minimizing the thermal resistance and thermal capacitance are proved to be the solutions to improve performance of FET in this paper.

Keywords

MOSFET, Short Channel Effect, Self-heating Effect, Strain

1. Introduction

In recent years, the scaling of CMOS circuits is getting smaller and smaller, to an extreme scale. As the scaling is reaching 3nm, the traditional technology is facing challenges and physical confinements. To improve the performance of FET in smaller scales, some new technologies must be applied. In this paper, we are going to explore innovations in terms of structures of FET and materials of FET that can improve the performances of FET.

The latest structure that is capable of improving the performance of FET in extreme small scale (3nm) is gate-all-around FET, also called GAAFET. This structure has stronger ability to limit short channel effect (SCE) in 3nm scale while finFET encounters more limitations as the scale gets smaller. In general, GAAFET has higher drive current and less time of delay than FinFET under the same scale.[1] However, GAAFET also faces challenges: heat dissipation. The temperature of GAAFET is higher than that of finFET under the same scale which is a major challenge for future development of GAAFET technology. Our argument is that GAAFET can replace finFET in smaller scales with the heat dissipation problem properly addressed.

If we still focus on FinFET, modifying material is a possible way to improve its performance. In terms of material, we mainly focus on strain engineering: applying stress (by changing the dopants) to improve mobility of carriers.[2] This method can change the configuration of electrons in silicon atoms which reduces effective mass and scattering. We are going to explore two strained structures using germanium: Si on Ge and SiGe S/D epitaxy. We also included simulations of strained FinFET to show the effectiveness of strain engineering.

2. Modifying structure to improve FinFET performance

2.1. GAAFET's Structural Advantage in Controlling Short Channel Effect

To show the structural modification in FETs, we first compare the contact area between gate and channel of planer FET, FinFET, and GAAFET. In Planar FET, there's only one interface which is the

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bottom of the gate. In FinFET, the contact area between gate and channel is largely increased: there are three interfaces between channel and gate as shown in fig 1.

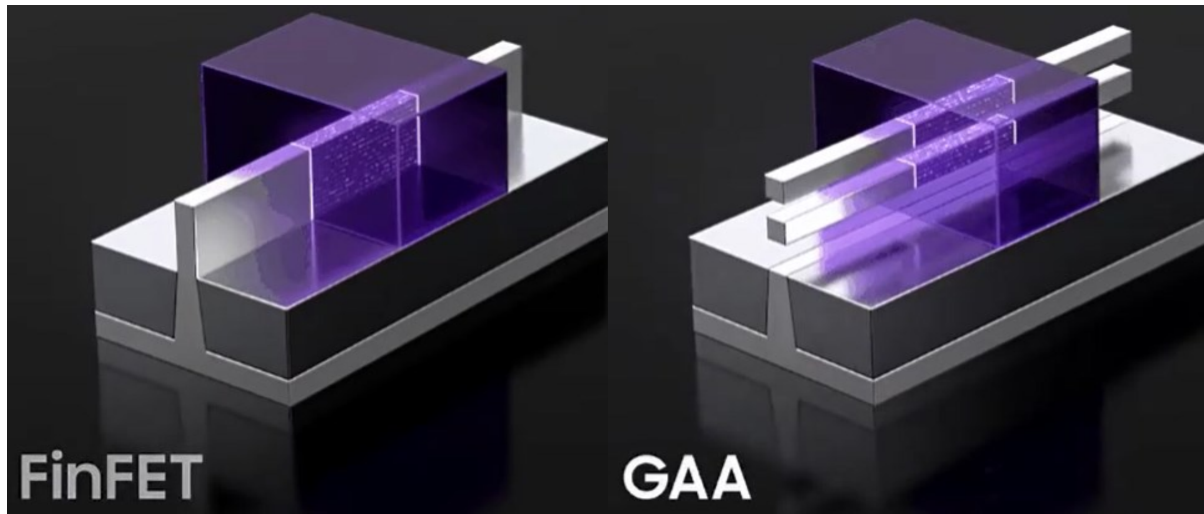

Figure 1: FinFET perspective view[3] **Figure 2:** GAAFET perspective view[3]

In GAAFET, the channel is surrounded by the gate (as shown in fig 2) which means there are four interfaces between the gate and channel. That's why it is called gate-all-around FET. It looks like the fin on FinFET is cut horizontally into several nanowires which forms the channel of GAAFET. As a result, the contacting area of GAAFET is even greater than FinFET.

The ranking of the contact area between channel and gate is: GAAFET > FinFET > Planar FET.

The ranking of control of gate over channel also follows this sequence because larger contacting area between channel and gate means greater control of gate over channel. GAAFET has greatest contacting area between gate and channel which means GAAFET's gate has better control over channel. Compared to GAAFET, FinFET encounters barriers in further limiting short channel effect. In FinFET, the prevalent method is to reduce fin width which can enhance the control of the gate[4].However, too thin fin width will cause scattering, resulting in reduction of the density of available states in the band edge, which means carriers would need more energy to occupy states in the conductive band[4]. Modifying its structure by moving to GAAFET is a reliable solution. In general, GAAFET has better structure to overcome short channel effect[5].

2.2. Comparing the performance of FinFET and GAAFET

In GAAFET, the short channel effect is better controlled which results in better control over drain-induced barrier lowering(DIBL). DIBL means applying drain bias to lower the energy barrier between source and channel so electrons can easily flow into the channel. DIBL will reduce the difference between "on" and "off" states. Better control of DIBL enables higher drive current with leakage current unchanged[1]. Since delay is given by CV/I(capacitance*voltage/current), with higher drive current, the switching speed is faster[1]. The working voltage of FET is also lowered due to better subthreshold swing and better control of DIBL[1]. However, the series resistance in GAAFET is greater, the drive current is reduced which means drive current in GAAFET is comparable to drive current in FinFET[1].

The table below shows performance of FinFET and GAAFET:

Table1

comparison of drive current (Ion), subthreshold swing (SS), drain-induced barrier lowering(DIBL), turn-on voltage(Vt), capacitance(C), and delay(CVt) between PFFET(FinFET) and GAAFET Ion vs. Leff and CV/I vs. Leff

	I_{on} (μA)	SS (mV/dec)	DIBL (mV/V)	V_t (mV)	C (10^{-17}F)	CV_t (ps)
PFFET	41.60	76.45	65.46	132	2.865	0.413
GAAFET	41.20	67.58	21.82	110	2.834	0.404

	I_{on} (μA)	SS (mV/dec)	DIBL (mV/V)	V_t (mV)	C (10^{-17}F)	CV/I (ps)
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GAAFET	42.10	67.58	21.82	110	2.834	0.404

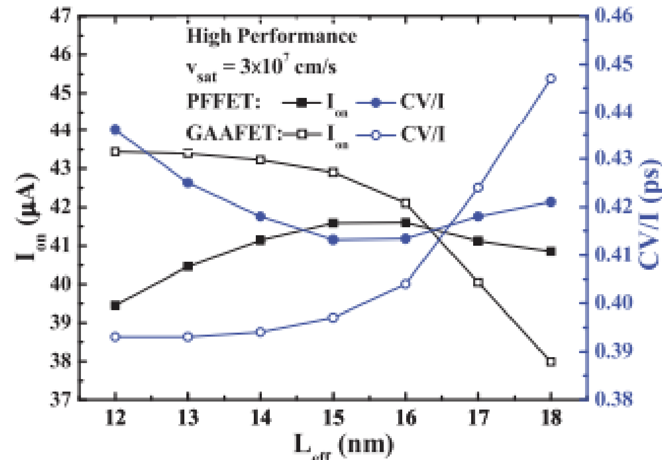

Figure 3: graph of drive current, I_{on}, and delay, CV/I, changing with effective length of the FET. Leff: effective channel length, Ioff=10nA[1]

According to the Figure 3, delay of GAAFET is lower and drive current is greater when effective channel length is less than 16nm. GAAFET is better at lower effective channel length.

2.3. Further improvements in shape of GAAFET

To further improve the performance of GAAFET, corner effects should be addressed. Corner effect has more influence on performance of GAAFET than that of FinFET.[6] To avoid corner effects, channels can be made into a more spherical shape.[5] The electric field is distributed more evenly in the spheric nanowire as shown in fig 4.

For a channel with diameter of 7 nanometers with a 2-nanometer-thick oxide layer, the subthreshold leakage current in the cylindrical channel is 1/5 time of the square shaped channel.[5]

Apart from avoiding channel effect, there are other structural considerations. For example, is nanosheet FET better than nanowire FET since it has greater sectional area which lowers series resistance? Does nanosheet FET have lower parasitic capacitance than nanowire ones? These are directions for future research in the shape of GAAFET.

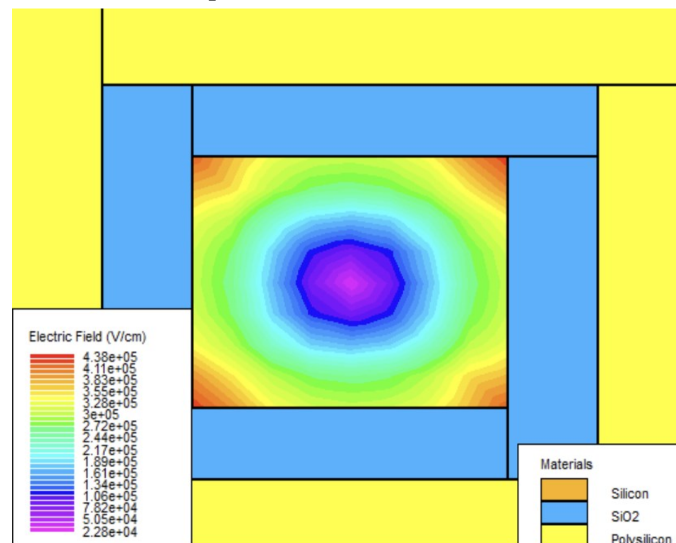

Figure 4: electric field distribution in rectangular channel and spheric channel [5]

2.4. Challenge: Self-Heating Effect

When electric current passes through a transistor, the kinetic energy of flowing electrons in a semiconductor is converted to thermal energy, heat. The self-heating effect defines such unwanted heat in the system. In general, the electrical conductivity decreases as temperature rises exponentially in semiconductors. The rise of thermal energy cases disabled the function of transistors, also sharply shortening the lifespan of transistors. Therefore, researchers are devoted to minimizing the self-heating effect or at least reducing the self-heating effect in an acceptable range.

Shortening the channel region is required to minimize the self-heating effect. Examined by Chuntaek Park and Ilgu Yun by applying different channel lengths to GaaFET under 5 GHz frequency, Fig 5 shows that the normalized thermal time constant (τ TH) increases with channel width. The thermal time constant is defined as the product of thermal resistance (R TH) and thermal capacitance (C TH). From the graph, normalized thermal resistance has a clear pattern to decrease with channel width while normalized thermal capacitance decreases with channel width. As a result of such two opposite characteristics, to minimize the self-heating effect is to look for the max product of thermal resistance and thermal capacitance.

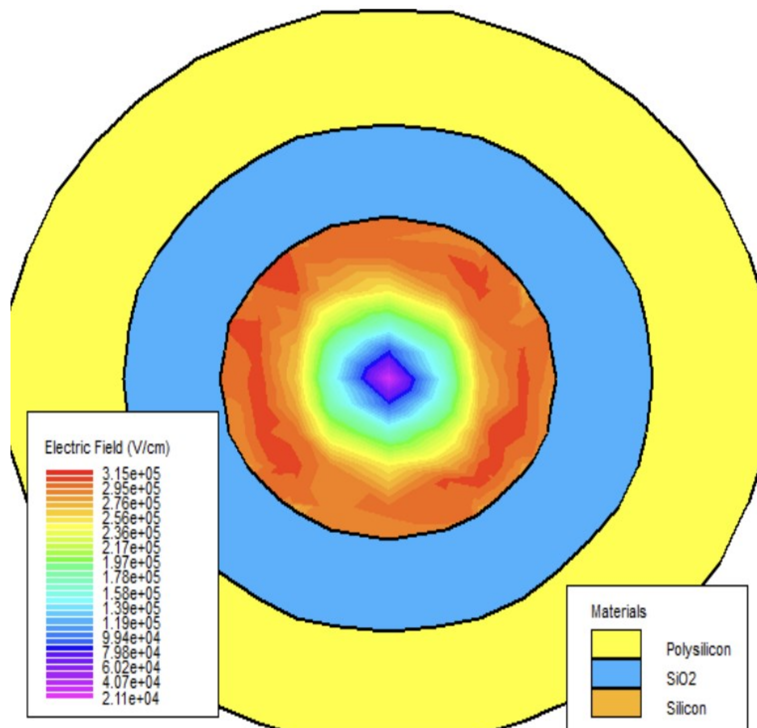

Figure 5: thermal time constant vs. channel width [7]

However, shortening the channel can potentially lead to a short channel effect. Therefore, it is important to find a balance between the limiting heat effect and the short channel effect.

3. Strain engineering to improve FinFET performance

3.1. About strain engineering

This part will have a brief review of the modern FinFET(Fin-shaped Field Effect Transistor) fabrication process and the strained structure in FinFET. Through integrated process optimization [8,9] and interfacial layer engineering [10], the performance advantages of SiGe channel on Si-pFETS can be realized. And how does the strain make the crystal lattice displace is shown in figure 6. Strain engineering can improve the performance of FinFET devices by applying stress to improve mobility (reduce effective mass and reduce scattering)

$$\mu = q\frac{\tau}{m^*} \tag{1}$$

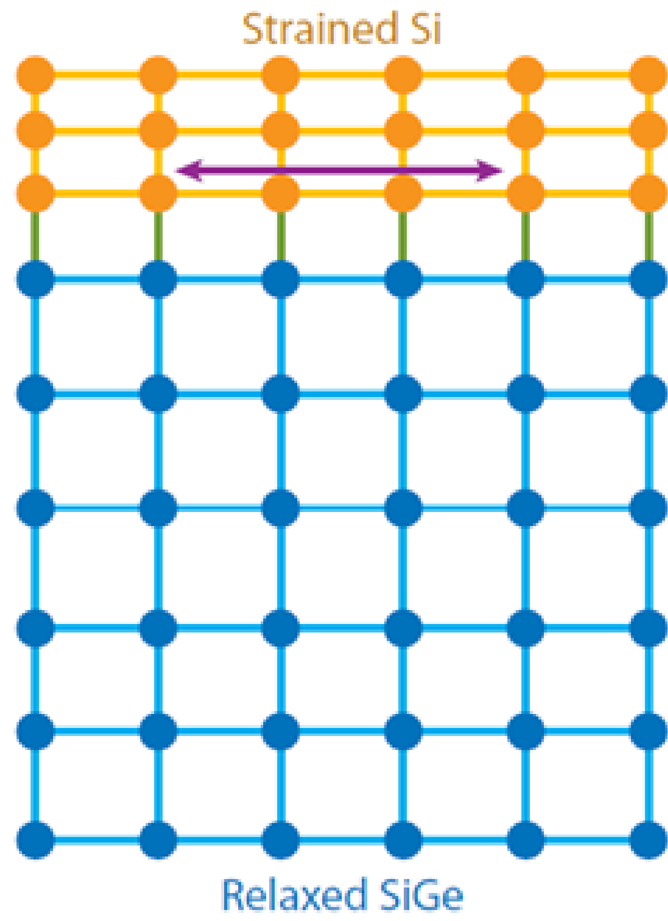

Figure 6: Strain in crystal lattice

3.2. Strained FinFET manufacture process

The process of fabrication are mentioned on the figure 7 and 8 before respectively. And the related manufacturing processes are dope, deposition, lithography, implantation, planarization and etching. The fabrication of modern FinFET is very complicate, and the parameter of each step is also in a dominant position for getting an ideal performance of transistors and the excellent performance of IC.

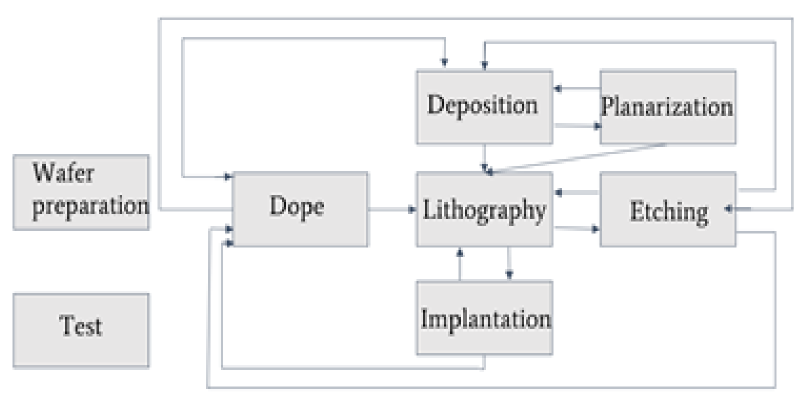

Figure 7: Strained FinFET fabrication process

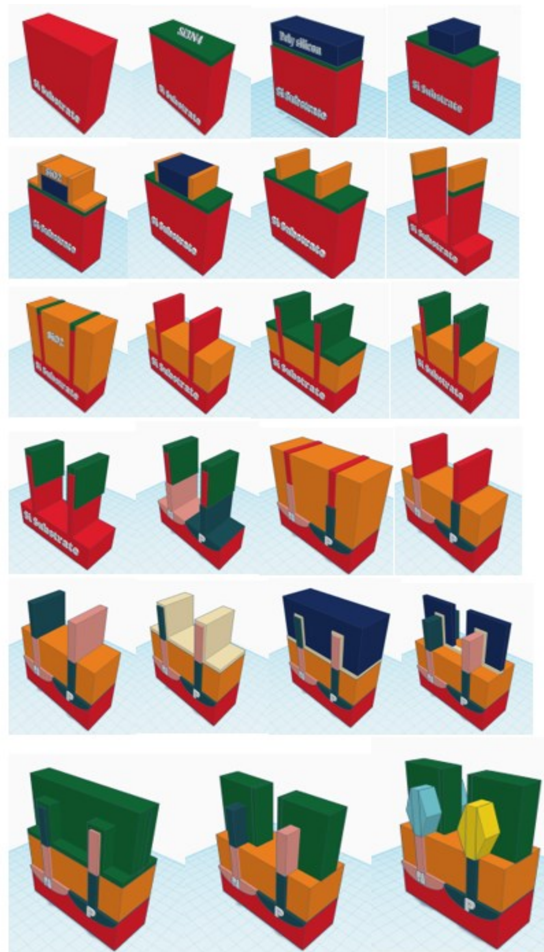

Figure 8: Strained FinFET fabrication process

3.3. Two kinds of strained structures

Stress/Strain technique is one of the promising techniques among many technologies for FinFETs with different piezo materials and high-k/metal gates. Recently, the dual strain Si/SiGe channel FinFET fabricated on the strain relaxation buffer (SRB) layer, it includes tensile strain Si-nFET and compression strain SiGe-pFET, have been proven to enhance electrons and holes mobility under the node of 7nm technology [11]. Two strained structures have been proved for the improvement of FinFET.

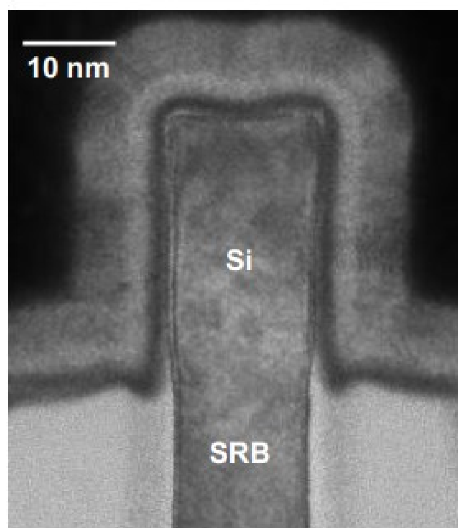

Figure 9: Si on SiGe SRB[12]

The first strained silicon structure applied to FinFET is Si on SiGe SRB (stress relaxed buffer), as shown in figure 9 [12]. The structure is a FinFET with SRB under the fin-shaped channel, and SiGe SRB could apply stress to the channel to make the device work more excellent. However, because of the difficulty of decoupling the strain in the channel, it is not completely explored for the contribution of the channel strain to the mobility of holes and electrons.

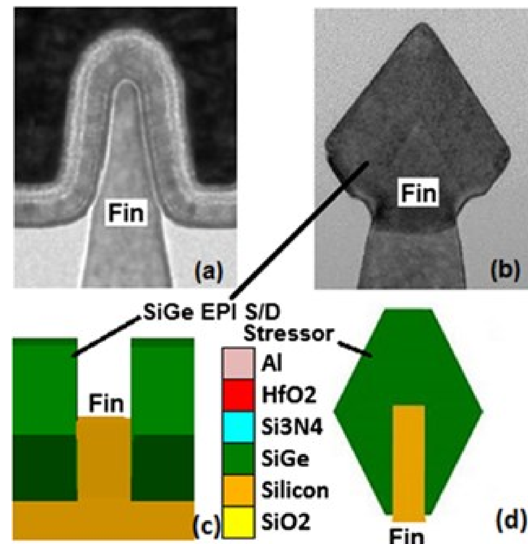

Figure 10: SiGe S/D epitaxy

The second structure is shown in figure 10. It is a FinFET with SiGe S/D epitaxy. The material of the source epitaxy layer and drain epitaxy layer is SiGe. And also the fraction of Ge content in SiGe determines the improvement for device performance. It has been verified in some research these days [13].

In conclusion, both SRB and S/D epitaxy layers can boost the performance of modern FinFET. In the next part, the discussion is about the quantitative representation of device performance improvement.

3.4. Simulations of strained FinFET

3.4.1. Introdution

In this section, I will discuss the performance optimization of the strain engineering finfet

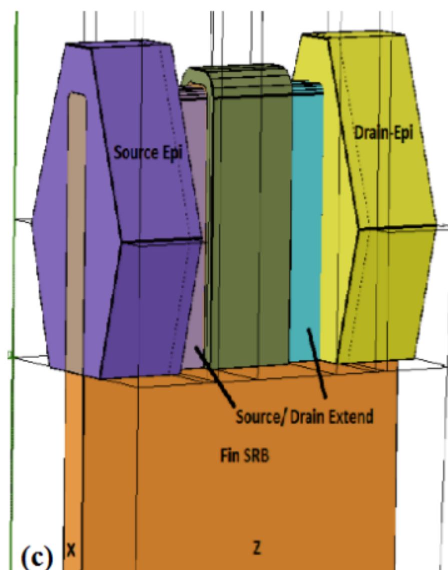

Figure 11: Structure of strained FinFET in simulation[14]

The research and simulation is based on a FinFET with both S/D epitaxy and SiGe SRB(stress relaxed buffer). And the parameters are shown below, the structure of the strained FinFET is also shown in fig 11. This FinFET is fabricated on Si substrate and it has Si0.9Ge0.1 SRB under the fin, and also with Source and Drain epitaxy layer surrounded. They have simulated the 3D displacement profile (amount of strain) for different Ge content and obtained the optimum result at Ge mole fraction of 0.3 because of high mobility.

3.4.2. Results and conclusions

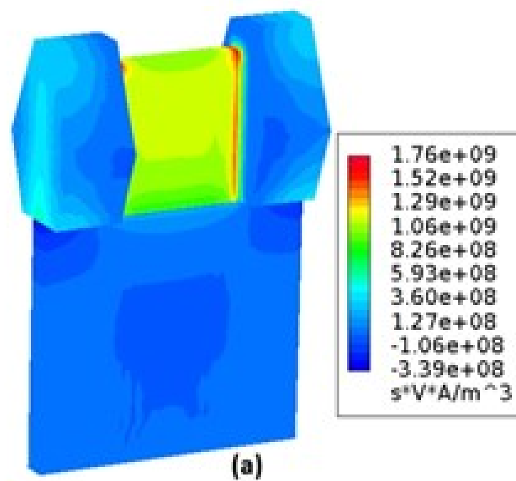

Figure 12: Stress distribution characteristics of n-FinFET, [13]

In this part, the simulation result will be discussed and also the conclusion. Figure 12 shows a 3D contour map of the stress distribution profile along the channel region, and for different Ge contents in the fin SRB, the one-dimensional stress distribution profile along the FinFET channel. Since the increase in Ge content leads to lattice mismatch and the effective carrier quality decreases, the mobility of the SiGe-based fin SRB region increases [15,16]. This enhances the carrier mobility of the Si channel at a higher Ge content [17].

Table 2
Electrical parameters of the simulation

% of Ge	Electrical parameter	Linear Region at V_D = 50mV	Saturation Region at V_D = 0.7V
0%	V_{TH}	213.389	199.214
	I_{off}	0.0145	0.0269
	I_{on}	20.9	0.0568
	SS	71.214	70.536
10%	V_{TH}	178.15	165.201
	I_{off}	0.0436	0.0849
	I_{on}	50.9	152
	SS	63.935	66.214
30%	V_{TH}	155.761	131.445
	I_{off}	0.159	0.299
	I_{on}	91.7	258
	SS	65.325	66.214

According to their simulation. The electrical parameters are shown in Table 2. When the content of Ge is 0%, in linear region at V_D =50mV, v_{TH} =213.389mV, I_{Off} =0.0145nA, Ion =20.9μA, SS=71.214mV/dec, in saturation region at V_D =0.7V, v_{TH} =199.214mV, I_{Off} =0.0269nA, Ion =0.0568μA, SS=70.536mV/dec.

When the content of Ge is 10%, in linear region at V_D=50mV, v_{TH}=178.15mV, Ioff=0.0436nA, Ion =50.9μA, SS=63.935mV/dec, in saturation region at V_D=0.7V, $v_TH = 165.201mV$, I_{Off}=0.0849nA, Ion =152μA, SS=66.214mV/dec.
When the content of Ge is 30%, in linear region at V_D=50mV, v_{TH}=155.761mV, I_{Off}=0.159nA, Ion =91.7μA, SS=65.325mV/dec, in saturation region at V_D=0.7V, v_{TH}=131.445mV, I_{Off}=0.299nA, Ion =258μA, SS=66.214mV/dec.

By changing the Ge% in fin SRB, the electrical parameters of the above-mentioned devices, such as v_{TH}, I_{Off}, Ion, subthreshold slope (SS), and DIBL, are calculated. It is found that the key equipment parameters (such as SS and DIBL) of all equipment are consistent, which is closer to ITRS requirements. With a germanium content of 30%, the device showed relatively best results, and the high turn-off current found was affected due to the high turn-on current and other standardized parameter values. As the band gap of the S/D region decreases, DIBL decreases with the increase of Ge content, so the mobility increases, which leads to the decrease of DIBL. The extracted DIBL of different germanium content (such as 0%, 10% and 30%) were 25.94, 23.28 and 23.56 mV/V, respectively.

4. Conclusion

Toward extreme scaling of field-effect transistors, by modifying the structure and using strain material, FET performance can be improved by those two methods. GAAFET is a structure that has better control in SCE and DIBL than FinFET while more subject to self-heating effects. And strain material can improve the mobility of electrons or holes by applying force on crystal lattice which can also make FET performance better.

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